BYTE SLICING GRØSTL
Optimized Intel AES-NI and 8-bit Implementations of the SHA-3 Finalist Grøstl

Kazumaro Aoki\textsuperscript{1,\textdagger}, Günther Roland\textsuperscript{2}, Yu Sasaki\textsuperscript{1} and Martin Schläffer\textsuperscript{2}
\textsuperscript{1}NTT Corporation, Japan
\textsuperscript{2}IAIK, Graz University of Technology, Austria
martin.schlaeffer@iaik.tugraz.at

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Abstract: Grøstl is an AES-based hash function and one of the 5 finalists of the SHA-3 competition. In this work we present high-speed implementations of Grøstl for small 8-bit CPUs and large 64-bit CPUs with the recently introduced AES instructions set (AES-NI) to speed up their implementations. Since Grøstl does not use the same MDS mixing layer as the AES, a direct application of the AES instructions seems difficult. In contrast to previous findings, our Grøstl implementations using the AES instructions are currently by far the fastest known. To achieve optimal performance we parallelize each round of Grøstl by taking advantage of the whole bit width of the used processor. This results in implementations running at 12.2 cycles/byte for Grøstl-256 and 18.6 cycles/byte for Grøstl-512.

1 INTRODUCTION

In 2007, NIST has initiated the SHA-3 competition [National Institute of Standards and Technology, 2007] to find a new cryptographic hash function standard. 51 interesting hash functions with different design strategies have been accepted for the first round. Many of these SHA-3 candidates are AES-based and might benefit from the Intel AES new instructions set (AES-NI) [Gueron and Intel Corp., 2010] to speed up their implementations. In [Benadjila et al., 2009] those candidates which use the AES round transformation as a main building block have been analyzed and implemented using AES-NI. In that work, the authors claim that algorithms which use a very different MDS mixing matrix than AES are too distant from AES and that there is no easy way to benefit from AES-NI.

Since December 2010, Grøstl [Gauravaram et al., 2011] is one of 5 finalists of the SHA-3 competition and uses the same S-box as AES but a very different MDS mixing matrix. In this work we show that it is still possible to efficiently implement Grøstl using AES-NI. Moreover, our AES-NI implementation of Grøstl is the fastest known implementation of Grøstl so far. Furthermore, we present a self-byte sliced implementation strategy which allows to implement Grøstl very efficiently on both 8-bit and 128-bit platforms. We achieve very good performance for larger bit widths by optimizing the MDS mixing matrix computation of Grøstl and by computing multiple columns in parallel. The parallel computation of the whole Grøstl round is possible and if parallel AES S-box table lookups (using AES-NI or the vpaes implementation of [Hamburg, 2009]) are available.

The paper is organized as follows. In Section 2, we give a short description of Grøstl. In Section 3, we describe requirements and general optimization techniques of our byte sliced implementations. In Section 4, we show how to minimize the computational requirements for MixBytes, the MDS mixing layer of Grøstl. In Section 5, we present the specific details of the 8-bit and 128-bit implementations. Finally, we conclude in Section 6.

2 DESCRIPTION OF GRØSTL

The hash function Grøstl was designed by Gauravaram et al. as a candidate for the SHA-3 competition [Gauravaram et al., 2011]. In January 2011, Grøstl has been tweaked for the final round of the competition and we only consider this variant here. It is an iterated hash function with a compression function built from two distinct permutations $P$ and $Q$. *Parts of this work were done while the author stayed at TU Graz.*
which are based on the same principles as the AES round transformation [National Institute of Standards and Technology, 2001]. Grøstl is a wide pipe design with security proofs for the collision and preimage resistance of the compression function [Fouque et al., 2009]. In the following, we describe the Grøstl hash function and the permutations of Grøstl-256 and Grøstl-512 in more detail.

2.1 The Grøstl Hash Function

The input message $M$ is padded and split into blocks $M_1, M_2, \ldots, M_t$ of $\ell$ bits with $t = 512$ for Grøstl-256 and $t = 1024$ for Grøstl-512. The initial value $H_0$, the intermediate hash values $H_i$, and the permutations $P$ and $Q$ are of size $\ell$ as well. The message blocks are processed via the compression function $f$, which accepts two inputs of size $\ell$ bits and outputs an $\ell$-bit value. The compression function $f$ is defined via the permutations $P$ and $Q$ as follows:

$$f(H, M) = P(H \oplus M) \oplus Q(M) \oplus H.$$  

The compression function is iterated with $H_0 = IV$ and $H_i \leftarrow f(H_{i-1}, M_i)$ for $1 \leq i \leq t$. The output $H_t$ of the last call of the compression function is processed by an output transformation $g$ defined as $g(x) = \text{trunc}_n(P(x) \oplus x)$, where $n$ is the output size of the hash function and $\text{trunc}_n(x)$ discards all but the least significant $n$ bits of $x$. Hence, the digest of the message $M$ is defined as $h(M) = g(H_t)$.

2.2 The Grøstl-256 Permutations

As mentioned above, two permutations $P$ and $Q$ are defined for Grøstl-256. Both permutations operate on a 512-bit state, which can be viewed as an $8 \times 8$ matrix of bytes. Each permutation of Grøstl-256 consists of 10 rounds, where the following four AES-like round transformations are applied to the state in the given order:

- **AddRoundConstant (AC)** XORS a constant to one row of the state for $P$ and to the whole state for $Q$. The constant changes for every round.
- **SubBytes (SB)** applies the AES S-box to each byte of the state.
- **ShiftBytes (SH)** cyclically rotates the bytes of rows to the left by $\{0,1,2,3,4,5,6,7\}$ positions in $P$ and by $\{1,3,5,7,0,2,4,6\}$ positions in $Q$.
- **MixBytes (MB)** is a linear diffusion layer, which multiplies each column with a constant $8 \times 8$ circulant MDS matrix.

2.2.1 MixBytes

As the MixBytes transformation is the most run-time intensive part of Grøstl in our case, we will describe this transformation in more detail here. The MixBytes transformation is a matrix multiplication performed on the state matrix as follows:

$$A \leftarrow B \times A,$$

where $A$ is the state matrix and $B$ is a circulant MDS matrix specified as $B = \text{circ}(02,02,03,04,05,03,05,07)$ or by the following matrix:

$$B = \begin{pmatrix}
02 & 02 & 03 & 04 & 05 & 03 & 05 & 07 \\
07 & 02 & 02 & 03 & 04 & 05 & 03 & 07 \\
05 & 07 & 02 & 02 & 03 & 04 & 05 & 03 \\
03 & 05 & 07 & 02 & 02 & 03 & 04 & 05 \\
05 & 03 & 05 & 07 & 02 & 02 & 03 & 04 \\
04 & 05 & 03 & 05 & 07 & 02 & 02 & 03 \\
03 & 04 & 05 & 03 & 05 & 07 & 02 & 02 \\
02 & 03 & 04 & 05 & 03 & 05 & 07 & 02
\end{pmatrix}.$$  

The multiplication is performed in a finite field $F_{256}$ defined by the irreducible polynomial $x^8 + x^4 + x^3 + x + 1$. As the multiplication by 2 only consists of a shift and a conditional XOR in binary arithmetic, we will calculate all multiplications by combining multiplications by 2 and additions (XOR), e.g. $7 \cdot x = (2 \cdot (2 \cdot x)) \oplus (2 \cdot x) \oplus x$.

For more details on the round transformations we refer to the Grøstl specification [Gauravaram et al., 2011].

2.3 The Grøstl-512 Permutations

The permutations used in Grøstl-512 are of size $\ell = 1024$ bits and the state is viewed as an $8 \times 16$ matrix of bytes. The permutations use the same round transformations as in Grøstl-256 except for ShiftBytes: Since the permutations are larger, the rows are shifted by $\{0,1,2,3,4,5,6,11\}$ positions to the left in $P$. In $Q$ the rows are shifted by $\{1,3,5,11,0,2,4,6\}$ positions to the left. The number of rounds is increased to 14.

3 BYTE SLICED IMPLEMENTATIONS OF GRØSTL

In this section, we describe some requirements for the efficient parallel computation of the Grøstl round transformations. Due to the fact that MixBytes applies the same algorithm to every column of the state
we can ‘byte slice’ Grøstl. In other words, we apply
the same computations for every byte-wise column of
the Grøstl state. On platforms with register sizes
larger than 8-bit we can parallelize every transforma-
tion by placing several bytes of one row (of the state)
inside one register. One column of the state is then
distributed over 8 different registers (see Figure 1).

![Figure 1: For the AES-NI implementation, the Grøstl-256
state is stored row-wise in xmm registers to compute each
column 16 times in parallel.](image)

3.1 Transposing the State

Unfortunately, the byte mapping in Grøstl is exactly
the opposite of this requirement. The state is mapped
to a byte sequence column-wise. Therefore we have
to transpose each input state to get bytes of the same
row into one register.

Once this realignment is done we can apply the
same operations on each column (or byte) stored in
the row registers at once. Even SubBytes which only
reorders the bytes of one row, is easier to implement
this way, because no data has to be moved between
registers.

3.2 AddRoundConstant

In AddRoundConstant a constant is XORed to the
state. This constant is different for P and Q and changes every round. When using large registers,
these constants can be precomputed and XORed row-
by-row and in parallel to each column of the state.

3.3 SubBytes

In order to improve the performance of the SubBytes
layer, we need to compute as many parallel S-box
lookups as possible.

In general, there is no easy way to lookup and re-
place each byte of a register using generic instructions
on large platforms. For this reason the T-table based
implementations are currently still the fastest on most
bigger platforms. However, the AES new instruc-
tions set gives us the possibility of 16 parallel S-box
lookups within only one instruction (see Section 5).

Another approach for parallel AES S-box table
lookups is to use small Log tables to efficiently com-
pute the inverse of the AES S-box using the vpaes
implementation presented in [Hamburg, 2009].

3.4 ShiftBytes

ShiftBytes is generally simple to implement on any
platform if the state is stored in row ordering. Only
byte shufflings, bitshifts and XORs, or addressing dif-
ferent state bytes (or words) is necessary.

3.5 MixBytes

As stated above, MixBytes is the transformation that
benefits most from byte slicing. MixBytes is computed using a large number of XORs and multiplica-
tions by two in \( \mathbb{F}_{256} \). The multiplication in the finite
field \( \mathbb{F}_{256} \) will be simplified to simple multiplications
by two and additions in \( \mathbb{F}_{256} \) (XORs).

For the multiplication by two we only need to shift
each byte to the left by one bit. To keep the result
in \( \mathbb{F}_{256} \) we have to observe the carry bit (MSB before
the shift operation). If the carry bit is zero the re-
sult is already correct (still in \( \mathbb{F}_{256} \)), if the carry bit is
one we have to reduce by the irreducible polynomial
(i.e. XOR 0x11B).

There are many strategies to reduce the number of
XOR computations for MixBytes and we discuss two
optimization strategies in detail in Section 4.

4 Optimizing the MixBytes Computation

The MDS matrix multiplication is the most complex
operation of Grøstl. Without optimizations all bytes
of a column have to be multiplied by 2, 3, 4, 5 and 7
and then summed up according to the following ma-
trix multiplication:

\[
\begin{bmatrix}
  b_0 \\
  b_1 \\
  b_2 \\
  b_3 \\
  b_4 \\
  b_5 \\
  b_6 \\
  b_7 \\
\end{bmatrix}
= \begin{bmatrix}
  2 & 2 & 3 & 4 & 5 & 3 & 5 & 7 \\
  7 & 2 & 2 & 3 & 4 & 5 & 3 & 5 \\
  5 & 7 & 2 & 2 & 3 & 4 & 5 & 3 \\
  3 & 5 & 7 & 2 & 2 & 3 & 4 & 5 \\
  5 & 3 & 5 & 7 & 2 & 2 & 3 & 4 \\
  4 & 5 & 3 & 5 & 7 & 2 & 2 & 3 \\
  3 & 4 & 5 & 3 & 5 & 7 & 2 & 2 \\
  2 & 3 & 4 & 5 & 3 & 5 & 7 & 2 \\
\end{bmatrix}
\begin{bmatrix}
  a_0 \\
  a_1 \\
  a_2 \\
  a_3 \\
  a_4 \\
  a_5 \\
  a_6 \\
  a_7 \\
\end{bmatrix}
\]

If we use only multiplications by 2 as described
above we can rewrite the same equations with factors
of only 2 and 4. See Listing 1. Without optimization,
the total number of XORs is \( 13 \cdot 8 = 104 \) and we need
16 multiplications by 2 (if we can store the results).
Note that a multiplication by 2 is usually about 3-5 times more expensive than an XOR operation.

\[ b_0 = a_2 \oplus a_3 \oplus a_5 \oplus a_6 \oplus a_7 \oplus 2a_0 \oplus 2a_1 \oplus 2a_2 \oplus 2a_3 \oplus 2a_5 \oplus 2a_7 \oplus 4a_3 \oplus 4a_4 \oplus 4a_6 \oplus 4a_7 \]

\[ b_1 = a_0 \oplus a_3 \oplus a_5 \oplus a_7 \oplus 2a_0 \oplus 2a_1 \oplus 2a_3 \oplus 2a_6 \oplus 4a_0 \oplus 4a_4 \oplus 4a_5 \oplus 4a_7 \]

\[ b_2 = a_0 \oplus a_1 \oplus a_4 \oplus a_5 \oplus a_7 \oplus 2a_1 \oplus 2a_2 \oplus 2a_3 \oplus 2a_4 \oplus 2a_6 \oplus 4a_0 \oplus 4a_2 \oplus 4a_5 \oplus 4a_7 \]

\[ b_3 = a_0 \oplus a_1 \oplus a_2 \oplus a_3 \oplus a_7 \oplus 2a_0 \oplus 2a_2 \oplus 2a_3 \oplus 2a_4 \oplus 2a_5 \oplus 2a_6 \oplus 2a_7 \oplus 4a_0 \oplus 4a_1 \oplus 4a_2 \oplus 4a_3 \oplus 4a_4 \oplus 4a_5 \]

\[ b_4 = a_0 \oplus a_1 \oplus a_2 \oplus a_3 \oplus a_4 \oplus 2a_1 \oplus 2a_2 \oplus 2a_3 \oplus 2a_4 \oplus 2a_5 \oplus 2a_6 \oplus 2a_7 \oplus 4a_0 \oplus 4a_1 \oplus 4a_2 \oplus 4a_3 \oplus 4a_5 \]

\[ b_5 = a_0 \oplus a_1 \oplus a_2 \oplus a_3 \oplus a_4 \oplus a_5 \oplus 2a_0 \oplus 2a_1 \oplus 2a_2 \oplus 2a_3 \oplus 2a_4 \oplus 2a_5 \oplus 2a_6 \oplus 2a_7 \oplus 4a_0 \oplus 4a_1 \oplus 4a_2 \oplus 4a_3 \oplus 4a_4 \oplus 4a_5 \]

\[ b_6 = a_1 \oplus a_3 \oplus a_4 \oplus a_5 \oplus a_6 \oplus 2a_0 \oplus 2a_1 \oplus 2a_2 \oplus 2a_3 \oplus 2a_4 \oplus 2a_5 \oplus 2a_6 \oplus 2a_7 \oplus 4a_0 \oplus 4a_1 \oplus 4a_2 \oplus 4a_3 \oplus 4a_4 \oplus 4a_5 \]

\[ b_7 = a_1 \oplus a_3 \oplus a_4 \oplus a_5 \oplus a_6 \oplus a_7 \oplus 2a_0 \oplus 2a_1 \oplus 2a_2 \oplus 2a_3 \oplus 2a_4 \oplus 2a_5 \oplus 2a_6 \oplus 2a_7 \oplus 4a_0 \oplus 4a_1 \oplus 4a_2 \oplus 4a_3 \oplus 4a_4 \oplus 4a_5 \oplus 4a_6 \]

Listing 1: MixBytes computation for one column with factors 1, 2 and 4. \( a_i \) are the input bytes and \( b_i \) are the output bytes.

### 4.1 Using Temporary Results

In this section, we show a MixBytes computation which tries to minimize the number of XORs and the used registers while keeping the minimum number of 16 multiplications by 2. This strategy is used for the Intel AES-NI implementation in Section 5.1.

Since many terms \((a_i \cdot 2 \cdot a_j \cdot a_k)\) in the computation are added to more than one result, we can save XORs by computing temporary results (see Table 1). For example, the term

\[
t = 2 \cdot a_0 + 2 \cdot a_2 + 1 \cdot a_5 + 4 \cdot a_7 + 1 \cdot a_7
\]

needs to be added to \(b_0\), \(b_1\), and \(b_3\). This has a total cost of 3 \(\cdot 5 = 15\) XORs using the naive approach. If we first compute the temporary result \(t\) and then add \(t\) to each of \(b_0\), \(b_1\), and \(b_3\), we can save \(15 - (4 + 3) = 8\) XORs.

There are many possibilities to compute temporary results and we used a greedy approach to find a good sequence. In each step of this approach, we try out all possible temporary results and compute the number of XORs we can save. In the first step, the maximum number of XORs we can save is 8. After we remove the already added terms, we continue with the greedy approach until only single terms are left.

Using this approach we found a sequence of computing MixBytes which requires 58 XORs and 16 multiplications by two. This sequence is shown by Table 1 and we use superscript numbers to denote the order of computing temporary results.

### 4.2 Reusing Results of \( \cdot 1 \)

In this section, we show a different MixBytes optimization technique which might be faster if more registers are available. This technique has been used for the 8-bit AVR implementation (see Section 5.2).

In Table 2 we have separated the MixBytes computation for each factor \(a_i\), \(2 \cdot a_i\), and \(4 \cdot a_i\). We use superscript numbers to denote the order in which we compute temporary results again. The values marked with letters are added to the temporary results after computing the first (intermediate) results to further optimize the computation, e.g.:

\[
\begin{align*}
b_{1,1} &= a_0 \oplus a_3 \\
b_{6,1} &= b_{1,1} \\
b_{1,1} &= b_{1,1} \oplus a_6 \\
b_{4,1} &= b_{1,1}
\end{align*}
\]

In this version the values that are multiplied by 2 are not calculated from the original inputs \(a_i\) but from the results of the first part of the calculation \(b_{1,1}\). While this significantly reduces the number of XORs the number of multiplications increases from 16 to 24: instead of multiplying every byte of the column first by 2 and then again by 2 to get the values multiplied by 4, we need to multiply the intermediate values too.

Although the number of multiplications increases to 24 we only need 47 XOR operations. This variant has been used for the 8-bit implementation of Grøstl in Section 5.2.

### 4.3 Minimizing the Number of XORs

The previous technique leads to another method to minimize the number of instructions in MixBytes. Using Table 2, we can observe that for each result \(b_i\), many \(a_j \oplus a_{j+1}\) terms are needed for each factor of 1, 2 and 4. By computing temporary results \(t_i\), \(x_i\) and \(y_i\) we get the following optimized MixBytes computation formulas with \(i = \{0, \ldots, 7\}\):

\[
\begin{align*}
t_i &= a_i + a_{i+1} \\
x_i &= t_i + t_{i+3} \\
y_i &= t_i + t_{i+2} + a_{i+6} \\
b_i &= 2 \cdot (2 \cdot x_{i+3} + y_{i+7}) + y_{i+4}
\end{align*}
\]
These formulas contain a minimum number of \(8 \cdot 2 = 16\) multiplications by 2 and in total, only \(8 \cdot 6 = 48\) XOR operations. However, it is still an open problem to find the smallest number of XORs needed to compute MixBytes of Grøstl. This strategy is also used for the Intel AES-NI implementation in Section 5.1. Note that this variant can also be used to improve Grøstl on the 8-bit platform.

## 5 IMPLEMENTATIONS

In the following we will describe specific implementation details for both the Intel AES-NI and 8-bit AVR platforms.

### 5.1 Intel AES-NI

Intel Processors based on the microarchitecture code-name Westmere come with a new AES instructions set (AES-NI) [Gueron and Intel Corp., 2010]. This set consists of six new instructions used for AES encryption and decryption. Next to improving the performance of AES they also provide more security due to their constant-time execution by avoiding cache-based table lookups. Furthermore, all processors with AES-NI come with different versions of SSE which we will also use to improve our implementations. For more information about the instructions used in this document we refer to the Intel Manual [Intel Corp., 2010].

Since Grøstl uses the same S-box as AES we can use AES-NI to improve the performance of Grøstl significantly. The implementation requires the processor to run in 64-bit mode to have access to the 16 128-bit XMM registers. This helps to avoid unnecessary memory accesses that would significantly reduce the performance. These 16 128-bit XMM registers provide enough space for the whole Grøstl state. Critical parts of the AES-NI implementation of Grøstl are written in assembler. In the following, we will discuss the main principles of the implementation and important observations.

### 5.1.1 State Alignment in Registers

For optimal performance, the alignment of the state inside the XMM registers is crucial. We have found that the best solution for Grøstl-256 is to compute P and Q simultaneously and put one row (64-bit) of each state side by side in one 128-bit XMM register. We then need 8 XMM registers to store both states. Thanks to MixBytes having the same MDS matrix for P and Q we can apply an optimized MixBytes algorithm to the whole XMM register and thus, to 16 columns of the state in parallel.

In Grøstl-512 we have 16 columns for each permutation which perfectly fit into 16 XMM registers. Hence, P and Q are computed separately and after each other but the same MixBytes algorithm can still be used 16 times in parallel again.

### 5.1.2 Transposing the State

To align the column-ordered message to fit the required row-ordering, the message has to be transposed after being loaded. For this purpose we use the PUNPCK instructions. The same has to be done with the IV for the initialization and in reverse order for the last chaining value before truncation. All the intermediate chaining values are kept in the transposed form.

In more detail, the PUNPCK instruction merges two XMM registers into one XMM register by interleaving the high or low bytes/words/doublewords or quadwords of the two source registers [Intel Corp., 2010]. A simple square matrix can be transposed using only PUNPCK instructions [Intel Corp., 1996]. As we initially have two 64-bit columns in each register, and

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### Table 1: MixBytes computation with 58 XORs. A “·” denotes those inputs \((a_i, 2 \cdot a_i, 4 \cdot a_i)\) which are added to get the results \(b_i\). Superscripts denote the order in which the temporary results are computed (1 corresponds to the temporary results of Equation 1).

<table>
<thead>
<tr>
<th>(a_0)</th>
<th>(a_1)</th>
<th>(a_2)</th>
<th>(a_3)</th>
<th>(a_4)</th>
<th>(a_5)</th>
<th>(a_6)</th>
<th>(a_7)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(b_0)</td>
<td>(a_0)</td>
<td>(a_0)</td>
<td>(a_0)</td>
<td>(a_0)</td>
<td>(a_0)</td>
<td>(a_0)</td>
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</tr>
<tr>
<td>(b_1)</td>
<td>(a_4)</td>
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<td>(a_4)</td>
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<tr>
<td>(b_2)</td>
<td>(a_6)</td>
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<tr>
<td>(b_3)</td>
<td>(a_8)</td>
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<td>(b_4)</td>
<td>(a_{10})</td>
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<td>(b_5)</td>
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<td>(b_6)</td>
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</tbody>
</table>
Table 2: MixBytes computation separated for factor 1, 2 and 4. $a_i$ are the input and $b_j$ the output bytes. A "•" denotes those inputs $(a_i, 2\cdot a_i, 4\cdot a_i)$ which are added to get the intermediate results $b_{i,j}$. Superscripts denote the order in which temporary values are computed. Note that the results for factor 2 can be computed only by multiplying the results of factor 1 by 2 (e.g. $b_{0,1,2} = 2b_{1,1,2}$).

<table>
<thead>
<tr>
<th>$b_{0,1}$</th>
<th>$b_{0,2}$</th>
<th>$b_{1,1}$</th>
<th>$b_{1,2}$</th>
<th>$b_{2,1}$</th>
<th>$b_{2,2}$</th>
<th>$b_{3,1}$</th>
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<tbody>
<tr>
<td>$a_0$</td>
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</tr>
</tbody>
</table>

These instructions combined will take less than 3 cycles to compute with a latency of about 6 cycles [Fog, 2010].

5.1.5 ShiftBytes

We can use the PSHUFB instruction (SSSE3) to quickly reorder the bytes in the XMM registers for ShiftBytes. This instruction is even faster than a simple shift instruction. Furthermore the PSHUFB instruction of ShiftBytes can be combined with the PSHUFB instruction to correct ShiftRows for AESENCLAST.

Two PSHUFB instructions with constant masks can be merged by shuffling the first mask using the second mask:

\[ \text{pshufb xmm0, mask1} \]
\[ \text{pshufb xmm0, mask2} \]

is equal to:

\[ (\text{pshufb mask1, mask2}) \]
\[ \text{pshufb xmm0, mask1} \]

where the shuffled mask is again a constant. The new mask (mask1) can be precomputed. This way we can save one PSHUFB instruction and only need to store one constant.

5.1.6 MixBytes

With the new row ordering we can compute 16 columns in parallel in one pass. We have implemented both variants which need a minimum number of 16 multiplications by 2. Apart from the multiplications by 2, the first variant of Section 4.1 needs 8 MOV and 32 XOR operations without memory access, and 25 MOV and 26 XOR operations with memory access (33 MOV and 58 XOR operations in total). For the second variant given in Section 4.3, we need 11 MOV and 32 XOR operations without memory access, and 8 MOV and 16 XOR operations with memory access (19 MOV and 48 XOR operations in total).

In the following, we show different implementation variants of the multiplication by 2 which can be used to implement MixBytes.

\textbf{Multiplication by 2 in }F_{2^{56}}\text{ with SSE or similar.} \quad \text{If SSE is available, the code shown below can be used}
to calculate the multiplication in parallel. In this example $xmm1$ is multiplied by 2 and $xmm0$ will be lost (paddb is used instead of psllq because of the shorter opcode):

```
movdqa xmm0, xmm1
psrlw xmm1, 7
pand xmm1, 0x0101...01
pmullw xmm1, 0x1b1b...1b
paddb xmm0, xmm0
pxor xmm1, xmm0
```

### Multiplication by 2 in $F_{256}$ with PBLENDVB

If SSE 4.1 is available we can use the PBLENDVB instruction to slightly speed up the algorithm described above. PBLENDVB merges two XMM registers into one. The source register is selected by the MSB of each byte in a third register. The MSB is also the bit that decides whether or not it is necessary to reduce the byte after shifting. Therefore we can use this instruction to generate a mask to XOR 0x1B where necessary. The multiplication as implemented is shown below where $xmm2$ is multiplied by 2, $xmm0$ and $xmm1$ are lost:

```
movdqa xmm0, xmm2
pand xmm2, 0x1b1b...1b
pxor xmm1, xmm1
paddb xmm2, xmm2
pblendvb xmm1, 0x7f7f...7f
pxor xmm2, xmm1
```

### Multiplication by 2 in $F_{256}$ with PCMPGTB

We get the fastest implementation using the PCMPGTB instruction. PCMPGTB compares signed bytes. If the MSB is set, the comparison with zero results in 0xFF and in 0x00 otherwise. The multiplication is shown below where $xmm1$ will be multiplied by 2, $xmm0$ will be lost and $xmm2$ has to be all 0x1B.

```
pxor xmm0, xmm0
pcmpgtb xmm0, xmm1
paddb xmm1, xmm1
pand xmm0, xmm2
pxor xmm1, xmm0
```

If ALU instructions are the bottleneck in the MixBytes implementation, we can also replace some instructions by their memory variant and get for example:

```
movaps xmm0, 0x0000...00
pcmpgtb xmm0, xmm1
paddb xmm1, xmm1
pand xmm0, 0x1b1b...1b
pxor xmm1, xmm0
```

### 5.1.7 Further Optimizations

For even higher performance we tried different local optimization techniques. We

- tried different variants of the MixBytes computation
- unrolled loops
- used precomputed constants for AddRoundConstant
- analyzed different instruction orders to improve parallel executions in different ALUs (micro-ops)
- used equivalent instructions with smaller opcode where possible
- tried different variants for the multiplication by 2
- used different variants of equivalent LOAD/STORE or ALU instructions to keep all units busy

While unrolling loops works perfectly for Grøstl-256, we found that unrolling all loops in Grøstl-512 increases the code size to exceed the cache size of the used CPU. This causes an immense drop in performance. Therefore using loops is necessary in this implementation.

### 5.1.8 Log Tables (vpaes)

As presented in [Hamburg, 2009], there is another way to compute the S-box relatively fast and cache-timing resistant without the use of AES instructions. By using Log tables to calculate inverses in $F_{2^4}$ it is possible to compute the inverse in $F_{2^8}$. This way the S-box can be realized with only 4-bit table lookups. These lookups can be implemented with PSHUFB instructions. Recently, Grøstl has been implemented this way in [Čalik, 2010]. We have implemented the AES S-box computation and improved the previous results using our optimized MixBytes computations. Note that the resulting vpaes implementation is now as fast as the T-table based implementation.

### 5.1.9 Intel AVX

The next generation of Intel processors feature a 256-bit extension to SSE called AVX. Using these new registers the possible bandwidth for parallel computations can be doubled. Even though PSHUFB and AESNCLAST will not be available for 256-bit registers, Grøstl-512 might run up to 50% faster because MixBytes and AddRoundConstant can be applied to P and Q at the same time.

### 5.1.10 Benchmarks

The final round version of Grøstl has been benchmarked on an Intel Core i7-620LM and Intel Core2 Duo L9400. For comparison, we also show benchmarks of the T-table implementation and the vpaes implementation. The results are shown in Table 3.
Table 3: Speed of the Grøstl AES-NI and vpaes implementations in cycles/byte on an Intel Core i7-M620 and Intel Core2 Duo L9400 processor (v1: using MixBytes computation of Section 4.1; v3: using MixBytes computation of Section 4.3).

<table>
<thead>
<tr>
<th>CPU</th>
<th>Version</th>
<th>Grøstl-256</th>
<th>Grøstl-512</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core i7</td>
<td>aesni v3</td>
<td>12.2</td>
<td>18.6</td>
</tr>
<tr>
<td></td>
<td>aesni v1</td>
<td>13.0</td>
<td>18.6</td>
</tr>
<tr>
<td></td>
<td>vpaes v1</td>
<td>23.2</td>
<td>32.6</td>
</tr>
<tr>
<td></td>
<td>(T-tables)</td>
<td>24.0</td>
<td>35.9</td>
</tr>
<tr>
<td>Core2</td>
<td>vpaes</td>
<td>21.2</td>
<td>29.2</td>
</tr>
<tr>
<td>Duo</td>
<td>(T-tables)</td>
<td>20.4</td>
<td>30.3</td>
</tr>
</tbody>
</table>

5.2 8-bit AVR (ATmega163)

The ATmega163 is an 8-bit microcontroller with 32 8-bit multi-purpose registers, 1024 Bytes of SRAM and 16K of flash memory. The multi-purpose registers can be used to manipulate data. The controller needs 2 cycles to read from and write to the SRAM and 3 cycles to read from flash memory. Six of the 8-bit registers are used as 16-bit address registers X, Y and Z, thus they can usually not be used for computations. For a list of instructions see [Atmel, 2003].

Because of the limited bit width of the architecture we can only compute one column at once. Therefore the most important part of the 8-bit optimization is minimizing the number of XORs in MixBytes as described above. With 26 available general purpose registers we have just enough space to keep the intermediate values loaded at all times during the computation of one column. All the other columns have to be written back to RAM.

The multiplication in $\mathbb{F}_{256}$ can be implemented with the code shown in Listing 2, where $r0$ is multiplied by 2, $r1$ has to be pre-set to 0x1B and $r2$ will be lost. These instructions will take 4 cycles to process.

```
LSL r0  # r0 = r0 << 1
IN r2, 0x3F # r2 = status register
SBRC r2, 0 # skip next if no carry
EOR r0, r1 # r0 = r0 + 0x1B
```

Listing 2: Multiplication by 2 for 8-bit version.

5.2.1 Benchmarks

We have implemented two different versions of the 8-bit implementation with the final round tweak (Grøstl) and three versions without the final round tweak (Grøstl-0) using different amounts of RAM. The versions are compared in Table 4.

<table>
<thead>
<tr>
<th>RAM</th>
<th>HighSpeed</th>
<th>Balanced</th>
<th>LowMem</th>
</tr>
</thead>
<tbody>
<tr>
<td>994</td>
<td>469</td>
<td>530</td>
<td>-</td>
</tr>
<tr>
<td>226</td>
<td>456</td>
<td>517</td>
<td>738</td>
</tr>
<tr>
<td>164</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4: Speed of three different Grøstl-256 8-bit AVR implementations in cycles/byte on an ATmega163. The last line shows the RAM usage in bytes (using MixBytes computation of Section 4.2).

6 CONCLUSION

In this work we have proposed two optimized algorithms for MixBytes, the MDS mixing layer of Grøstl, which allow to speed up Grøstl on various platforms. Furthermore, byte slicing provides the possibility to parallelize the Grøstl computation if the registers are large enough and parallel AES S-box table lookups are available. This is the case for Intel processors including the new AES instructions set or in general, using the vpaes implementation.

Both implementations show that Grøstl can be implemented efficiently on very different platforms. The 8-bit implementation will run at 469 cycles per byte on this very limited target hardware. The AES-NI implementation shows that even though Grøstl is very different from AES it still can take advantage of these new instructions. More specifically, our Intel AES-NI implementation of Grøstl is the fastest known implementation so far. Grøstl-256 runs at about 12.2 cycles per byte on an Intel Core i7-M620, which is about 50% faster than the table-based version on the same CPU.

We have reduced the number of operation needed to compute MixBytes to only 48 XORs with 16 multiplications by 2. Future work includes the optimization of the MixBytes computation to take more advantage of the 3 available ALUs in current Intel processors by minimizing the dependency chains. Also future CPU features like AVX will provide another opportunity to increase the performance, especially for the larger variant Grøstl-512.
ACKNOWLEDGEMENTS

The authors thank Krystian Matusiewicz for useful discussions and for fine-tuning the AES-NI implementations. This work was supported in part by the European Commission through the ICT Programme under Contract ICT-2007-216646 ECRYPT II, by the Austrian Science Fund (FWF), project P21936 and by the IAP Programme P6/26 BCRYPT of the Belgian State (Belgian Science Policy).

REFERENCES


APPENDIX

The following tables show how the message block gets transposed. PUNPCK always interleaves the same half of two registers depending on the specific instruction used. For example PUNPCKLWD interleaves the lower half of the first input operand with the lower half of the second operand as words (16 bits), i.e. first word of operand 1, first word of operand 2, second word of operand 1, second word of operand 2 and so on.

To achieve the transposition needed for Grostl we first reorder the message bytes to get words of the same row next to each other, then unpack and interleave with the register containing the adjacent elements (e.g. A0-A1 and A2-A3). We then have to re-order again to get two rows that are next to each other in one register after the final PUNPCK.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>movaps xmm0, 0x0000 ...00</td>
<td>Move packed single-integer values from memory to the destination register</td>
</tr>
<tr>
<td>pcmpgtb xmm0, xmm1</td>
<td>Compare byte fields for greater-than</td>
</tr>
<tr>
<td>paddb xmm1, xmm1</td>
<td>Add packed single-integer values</td>
</tr>
<tr>
<td>pand xmm0, 0x1b1b ...1b</td>
<td>And packed single-integer values</td>
</tr>
<tr>
<td>pxor xmm1, xmm0</td>
<td>Exclusive-or packed single-integer values</td>
</tr>
</tbody>
</table>
### Table 5: Initial contents.

<table>
<thead>
<tr>
<th>XMM0</th>
<th>XMM1</th>
<th>XMM2</th>
<th>XMM3</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>A2</td>
<td>A4</td>
<td>A6</td>
</tr>
<tr>
<td>B0</td>
<td>B2</td>
<td>B4</td>
<td>B6</td>
</tr>
<tr>
<td>C0</td>
<td>C2</td>
<td>C4</td>
<td>C6</td>
</tr>
<tr>
<td>D0</td>
<td>D2</td>
<td>D4</td>
<td>D6</td>
</tr>
<tr>
<td>E0</td>
<td>E2</td>
<td>E4</td>
<td>E6</td>
</tr>
<tr>
<td>F0</td>
<td>F2</td>
<td>F4</td>
<td>F6</td>
</tr>
<tr>
<td>G0</td>
<td>G2</td>
<td>G4</td>
<td>G6</td>
</tr>
<tr>
<td>H0</td>
<td>H2</td>
<td>H4</td>
<td>H6</td>
</tr>
<tr>
<td>A1</td>
<td>A3</td>
<td>A5</td>
<td>A7</td>
</tr>
<tr>
<td>B1</td>
<td>B3</td>
<td>B5</td>
<td>B7</td>
</tr>
<tr>
<td>C1</td>
<td>C3</td>
<td>C5</td>
<td>C7</td>
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<tr>
<td>D1</td>
<td>D3</td>
<td>D5</td>
<td>D7</td>
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<tr>
<td>E1</td>
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<td>E5</td>
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<tr>
<td>F1</td>
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<tr>
<td>G1</td>
<td>G3</td>
<td>G5</td>
<td>G7</td>
</tr>
<tr>
<td>H1</td>
<td>H3</td>
<td>H5</td>
<td>H7</td>
</tr>
</tbody>
</table>

### Table 6: Reordering before `PUNPCK*WD`.

<table>
<thead>
<tr>
<th>XMM0</th>
<th>XMM1</th>
<th>XMM2</th>
<th>XMM3</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>C0</td>
<td>A4</td>
<td>C4</td>
</tr>
<tr>
<td>A1</td>
<td>C1</td>
<td>A5</td>
<td>C5</td>
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<tr>
<td>A2</td>
<td>C2</td>
<td>A6</td>
<td>C6</td>
</tr>
<tr>
<td>A3</td>
<td>C3</td>
<td>A7</td>
<td>C7</td>
</tr>
<tr>
<td>E0</td>
<td>G0</td>
<td>E4</td>
<td>G4</td>
</tr>
<tr>
<td>E1</td>
<td>G1</td>
<td>E5</td>
<td>G5</td>
</tr>
<tr>
<td>E2</td>
<td>G2</td>
<td>E6</td>
<td>G6</td>
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<tr>
<td>E3</td>
<td>G3</td>
<td>E7</td>
<td>G7</td>
</tr>
<tr>
<td>B0</td>
<td>D0</td>
<td>B4</td>
<td>D4</td>
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<tr>
<td>B1</td>
<td>D1</td>
<td>B5</td>
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<tr>
<td>B2</td>
<td>D2</td>
<td>B6</td>
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<tr>
<td>B3</td>
<td>D3</td>
<td>B7</td>
<td>D7</td>
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<tr>
<td>F0</td>
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<td>F4</td>
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<tr>
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<td>F3</td>
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<td>F7</td>
<td>H7</td>
</tr>
</tbody>
</table>

### Table 7: After `PUNPCK*WD`.

<table>
<thead>
<tr>
<th>XMM0</th>
<th>XMM1</th>
<th>XMM2</th>
<th>XMM3</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>C0</td>
<td>A4</td>
<td>C4</td>
</tr>
<tr>
<td>A1</td>
<td>C1</td>
<td>A5</td>
<td>C5</td>
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<tr>
<td>A2</td>
<td>C2</td>
<td>A6</td>
<td>C6</td>
</tr>
<tr>
<td>A3</td>
<td>C3</td>
<td>A7</td>
<td>C7</td>
</tr>
<tr>
<td>E0</td>
<td>G0</td>
<td>E4</td>
<td>G4</td>
</tr>
<tr>
<td>E1</td>
<td>G1</td>
<td>E5</td>
<td>G5</td>
</tr>
<tr>
<td>E2</td>
<td>G2</td>
<td>E6</td>
<td>G6</td>
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<tr>
<td>E3</td>
<td>G3</td>
<td>E7</td>
<td>G7</td>
</tr>
<tr>
<td>B0</td>
<td>D0</td>
<td>B4</td>
<td>D4</td>
</tr>
<tr>
<td>B1</td>
<td>D1</td>
<td>B5</td>
<td>D5</td>
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<tr>
<td>B2</td>
<td>D2</td>
<td>B6</td>
<td>D6</td>
</tr>
<tr>
<td>B3</td>
<td>D3</td>
<td>B7</td>
<td>D7</td>
</tr>
<tr>
<td>F0</td>
<td>H0</td>
<td>F4</td>
<td>H4</td>
</tr>
<tr>
<td>F1</td>
<td>H1</td>
<td>F5</td>
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</tr>
<tr>
<td>F2</td>
<td>H2</td>
<td>F6</td>
<td>H6</td>
</tr>
<tr>
<td>F3</td>
<td>H3</td>
<td>F7</td>
<td>H7</td>
</tr>
</tbody>
</table>

### Table 8: Reordering before `PUNPCK*DQ`.

<table>
<thead>
<tr>
<th>XMM0</th>
<th>XMM1</th>
<th>XMM2</th>
<th>XMM3</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>C0</td>
<td>A4</td>
<td>C4</td>
</tr>
<tr>
<td>A1</td>
<td>C1</td>
<td>A5</td>
<td>C5</td>
</tr>
<tr>
<td>A2</td>
<td>C2</td>
<td>A6</td>
<td>C6</td>
</tr>
<tr>
<td>A3</td>
<td>C3</td>
<td>A7</td>
<td>C7</td>
</tr>
<tr>
<td>E0</td>
<td>G0</td>
<td>E4</td>
<td>G4</td>
</tr>
<tr>
<td>E1</td>
<td>G1</td>
<td>E5</td>
<td>G5</td>
</tr>
<tr>
<td>E2</td>
<td>G2</td>
<td>E6</td>
<td>G6</td>
</tr>
<tr>
<td>E3</td>
<td>G3</td>
<td>E7</td>
<td>G7</td>
</tr>
<tr>
<td>B0</td>
<td>D0</td>
<td>B4</td>
<td>D4</td>
</tr>
<tr>
<td>B1</td>
<td>D1</td>
<td>B5</td>
<td>D5</td>
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<tr>
<td>B2</td>
<td>D2</td>
<td>B6</td>
<td>D6</td>
</tr>
<tr>
<td>B3</td>
<td>D3</td>
<td>B7</td>
<td>D7</td>
</tr>
<tr>
<td>F0</td>
<td>H0</td>
<td>F4</td>
<td>H4</td>
</tr>
<tr>
<td>F1</td>
<td>H1</td>
<td>F5</td>
<td>H5</td>
</tr>
<tr>
<td>F2</td>
<td>H2</td>
<td>F6</td>
<td>H6</td>
</tr>
<tr>
<td>F3</td>
<td>H3</td>
<td>F7</td>
<td>H7</td>
</tr>
</tbody>
</table>
Table 9: After PUNPCK*DQ.

<table>
<thead>
<tr>
<th>XMM0</th>
<th>XMM1</th>
<th>XMM2</th>
<th>XMM3</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>C0</td>
<td>E0</td>
<td>G0</td>
</tr>
<tr>
<td>A1</td>
<td>C1</td>
<td>E1</td>
<td>G1</td>
</tr>
<tr>
<td>A2</td>
<td>C2</td>
<td>E2</td>
<td>G2</td>
</tr>
<tr>
<td>A3</td>
<td>C3</td>
<td>E3</td>
<td>G3</td>
</tr>
<tr>
<td>A4</td>
<td>C4</td>
<td>E4</td>
<td>G4</td>
</tr>
<tr>
<td>A5</td>
<td>C5</td>
<td>E5</td>
<td>G5</td>
</tr>
<tr>
<td>A6</td>
<td>C6</td>
<td>E6</td>
<td>G6</td>
</tr>
<tr>
<td>A7</td>
<td>C7</td>
<td>E7</td>
<td>G7</td>
</tr>
<tr>
<td>B0</td>
<td>D0</td>
<td>F0</td>
<td>H0</td>
</tr>
<tr>
<td>B1</td>
<td>D1</td>
<td>F1</td>
<td>H1</td>
</tr>
<tr>
<td>B2</td>
<td>D2</td>
<td>F2</td>
<td>H2</td>
</tr>
<tr>
<td>B3</td>
<td>D3</td>
<td>F3</td>
<td>H3</td>
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<tr>
<td>B4</td>
<td>D4</td>
<td>F4</td>
<td>H4</td>
</tr>
<tr>
<td>B5</td>
<td>D5</td>
<td>F5</td>
<td>H5</td>
</tr>
<tr>
<td>B6</td>
<td>D6</td>
<td>F6</td>
<td>H6</td>
</tr>
<tr>
<td>B7</td>
<td>D7</td>
<td>F7</td>
<td>H7</td>
</tr>
</tbody>
</table>