ARMageddon: Last-Level Cache Attacks on Mobile Devices

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Abstract—In the last 10 years cache attacks on Intel CPUs have gained increasing attention among the scientific community. More specifically, powerful techniques to exploit the cache side channel have been developed. However, so far only a few investigations have been performed on modern smartphones and mobile devices in general. In this work, we describe Evict+Reload, the first access-based cross-core cache attack on modern ARM Cortex-A architectures as used in most of today’s mobile devices. Our attack approach overcomes several limitations of existing cache attacks on ARM-based devices, for instance, the requirement of a rooted device or specific permissions. Thereby, we broaden the scope of cache attacks in two dimensions. First, we show that all existing attacks on the x86 architecture can also be applied to mobile devices. Second, despite the general belief these attacks can also be launched on non-rooted devices and, thus, on millions of off-the-shelf devices.

Similarly to the well-known Flush+Reload attack for the x86 architecture, Evict+Reload allows to launch generic cache attacks on mobile devices. Based on cache template attacks we identify information leaking through the last-level cache that can be exploited, for instance, to infer tap and swipe events, inter-keystroke timings as well as the length of words entered on the touchscreen, and even cryptographic primitives implemented in Java. Furthermore, we demonstrate the applicability of Prime+Probe attacks on ARM Cortex-A CPUs. The performed example attacks demonstrate the immense potential of our proposed attack techniques.

I. INTRODUCTION

Cache attacks represent a powerful means of exploiting the different access times within the memory hierarchy of modern system architectures. Until recently these attacks explicitly targeted cryptographic implementations. The seminal paper of Yarom and Falkner [58], however, introduced the so-called Flush+Reload attack, which allows an attacker to infer which specific parts (instructions as well as data) of a binary (shared object or executable) are accessed by a victim program. Thereby, Flush+Reload allows more fine-grained attacks than previous approaches like, for instance, plain timing attacks [8], or the well-known Evict+Time and Prime+Probe techniques [42]. Recently, Gruss et al. [18] even demonstrated the possibility to use Flush+Reload to automatically exploit cache-based side channels by so-called cache template attacks on Intel platforms. Flush+Reload does not only allow for efficient attacks against crypto implementations (cf. [7], [24], [55]) but also to infer keystroke information and even to build keyloggers on Intel platforms [18]. Thus, cache attacks represent a significant threat to today’s computing platforms.

Although a few publications about cache attacks against AES T-table implementations on mobile devices exist (cf. [9], [49]–[51], [56]), the recent advances in terms of highly accurate and generic attacks have been demonstrated on x86 platforms only. More specifically, open challenges caused by the significant differences in terms of cache architecture and privileged instructions on modern x86 and ARM architectures have prevented these attacks from being mounted on ARM-based devices for years. Therefore, we investigate these open challenges in more detail and show that all of these issues can be overcome in practice. Thereby, we demonstrate that all existing cache attacks proposed for x86 architectures can also be applied on ARM architectures, which allows for real-world attack scenarios on millions of off-the-shelf Android devices without any special privileges or permissions.

As smartphones continue to evolve as the most important personal computing platform, the investigation of more generic cache attacks on mobile devices is of utmost importance. Based on related work in this area of research, we found that cache attacks are not practically relevant on ARM because of the following issues, which we overcome in this work.

1) Random replacement policy: The random replacement policy—used to replace specific cache lines within a cache set—has been mentioned as one possible source of noise in case of time-driven cache attacks [49], [51]. Furthermore, due to the random replacement policy, the Evict+Time approach is so far considered more appropriate than the Prime+Probe approach [50].

2) Precise timing: So far, precise timings on the ARM platform relied on the cycle count register (PMCCNTR) [3] that is only accessible in unprivileged mode if access is explicitly granted by a privileged application. Thus, these attacks assume that the Android device is rooted and the exploitation of cache attacks on non-rooted devices has been mentioned as an interesting open challenge [50].

3) Flush instruction: In contrast to Intel x86 platforms, ARM restricts the usage of dedicated flush instructions to privileged mode only. Thus, the device needs to be rooted and the attacker needs to permanently install a kernel module. However, an attacker can also perform cache eviction by accessing multiple congruent addresses
to evict all data from a specific cache set. Due to improved replacement policies previously published eviction is not practical anymore on more recent CPUs.

4) **Cache architecture:** One of the prerequisites of the **Flush+Reload** attack is an inclusive shared last-level cache. Inclusive means that data which is present in the lower cache levels, e.g., L1 cache, must also be present within higher cache levels and shared means that the last-level cache is shared among all cores. These properties allow any process to evict specific data from another core’s L1 cache. However, ARM Cortex-A processors did not support an inclusive shared last-level cache until the ARM Cortex-A53/A57 generation.

The above mentioned challenges show the significant differences between modern Intel platforms and ARM platforms. Eventually, we show how to tackle these challenges and our insights clearly demonstrate the feasibility of highly efficient cache attacks on ARM platforms. Thereby, we do not restrict our investigations to cryptographic implementations but also consider cache attacks as a means to infer inter-keystroke timings or the length of swipe actions. In addition, our investigations show that our attack approach allows a malicious application to determine when a specific library is used. For instance, the presented attack can be used to determine whether the GPS sensor is active, or whether other features like the microphone or the camera are used. This information further allows an adversary to infer privacy-sensitive information about the user.

We do not aim to list the possible exploits exhaustively but only demonstrate the immense attack potential of our proposed **Evict+Reload** attack. Given this powerful technique, we believe that many sophisticated cache attacks will be presented in the future. We address this to the fact that **Evict+Reload** can be used to scan any library or program binary for possible information leaks resulting from the cache side channel.

**Contributions.** The contributions of this work can be summarized as follows.

- We are the first to successfully perform highly efficient and accurate cache attacks on ARM CPUs, which so far have only been shown for x86 platforms. More specifically, we demonstrate that the **Evict+Reload** approach can be used to apply **Flush+Reload**-like attacks. Furthermore, we are the first to demonstrate the feasibility of **Prime+Probe** attacks on ARM. Our attacks are the first access-driven cache attacks that exploit the last-level cache and, thus, work across CPU cores.
- Our attack is the first to demonstrate that local instruction caches can be attacked via data memory accesses, even if the last-level cache is only inclusive on the instruction side but not on the data side.
- We show that cache-based covert channels significantly outperform existing covert channels on Android.
- We show that cache template attacks can be used to launch sophisticated attacks on mobile devices, including attacks against cryptographic implementations used in practice but also more fine-grained attacks like inter-keystroke timings and swipe actions on the touchscreen.

**Outline.** The remainder of this paper is structured as follows. In Section [II] we start with basic information about CPU caches and shared memory in general. Furthermore, we cover related work in this area of research. Section [III] presents a more realistic adversary model with fewer assumptions than existing attacks and identifies the challenges that need to be solved for such an adversary model. We describe the **Evict+Reload** attack in Section [IV] and we also state solutions to the previously identified challenges on ARM platforms. In Section [V] we evaluate the performance of a cross-core covert channel between two Android applications based on our **Evict+Reload** attack. In Section [VI] we demonstrate cache template attacks on Android based on our **Evict+Reload** approach. In Section [VII] we describe how the eviction from the **Evict+Reload** attack can be used to build a **Prime+Probe** attack. We discuss possible countermeasures against the identified weaknesses in Section [VIII] and we discuss interesting open research challenges in Section [IX]. Last but not least, we conclude this work in Section [X].

**II. BACKGROUND AND RELATED WORK**

In this section, we give a basic introduction to the concept of CPU caches and compare modern Intel CPU caches to modern ARM CPU caches. We discuss the basics of shared memory. Furthermore, we provide a basic introduction to cache attacks on ARM and Intel architectures.

A. CPU Caches

Today’s CPU performance is influenced not only by the clock frequency but also by the latency of instructions, operand fetches, and other interaction with internal and external devices. All CPU computations require data from the system memory, but reducing the latency of system memory is difficult. Instead, CPUs employ caches to buffer frequently used data in smaller and faster internal memories, effectively hiding the latency of slow accesses to the system memory.

Modern caches are organized in sets of cache lines, which is also known as set-associative caches. Each memory address maps to one of these cache sets and memory addresses that map to the same cache set are considered as being congruent. Congruent addresses compete for cache lines within the same set. Therefore, CPUs implement replacement policies, for example, least-recently used (LRU) eviction which is common on Intel CPUs. However, these replacement policies are widely undocumented [17].

CPU caches can be virtually indexed and physically indexed caches, which derive the index from the virtual or physical address, respectively. Virtually indexed caches are generally faster because they do not require virtual to physical address translation before the cache lookup. However, using the virtual address leads to the situation that the same physical address might be cached in different cache lines, which again introduces performance penalties. In order to uniquely identify the actual address that is cached within a specific cache line, a so-called tag is used. This tag again can be based on the virtual or physical address. Most modern caches use physical tags because they can be computed simultaneously to locating the cache set.

CPUs have multiple cache levels, with the lower levels being faster and smaller than the higher levels. If all cache lines from lower levels are also stored in a higher-level cache
line, we call the higher-level cache inclusive. If a cache line can only reside in one of the cache levels at any point in time, we call the caches exclusive. The last-level cache is often shared among all cores to enhance the performance upon transitioning threads between cores and to simplify cross-core cache lookups. However, with shared last-level caches that are exclusive or inclusive, one core can (intentionally) influence the cache content of all other cores. This is the basis for cache attacks such as the Flush+Reload \cite{58} attack.

In this paper we focus on two CPUs, a Qualcomm Krait 400 and an ARM Cortex-A53, both very common quad-core CPUs used in today’s smartphones.

The Qualcomm Krait 400 runs at 2.88 GHz. It has two 16 KB L1 caches—one for data and one for instructions—per core, with a cache line size of 64 bytes. The L1 caches are physically indexed and physically tagged and have 4 ways and 64 cache sets. The L2 cache is shared among all cores, but it is neither inclusive nor exclusive \cite{3}. The L2 cache has a size of 2 MB and is divided into 2 048 sets, each with 8 cache lines and a cache line size of 128 bytes.

The more recent ARM Cortex-A53 runs at 1.2 GHz. It has two 4-way 32 KB L1 caches—one for data and one for instructions—per core, with a cache line size of 64 bytes. The L1 caches are again physically indexed and physically tagged and have 128 cache sets. The L2 cache is shared among all cores and inclusive with respect to the L1 instruction cache but exclusive with respect to the L1 data cache. It has a total size of 512 KB and is divided into 512 sets with 16 cache lines each and a cache line size of 64 bytes.

### B. Shared Memory

While writeable shared memory can be used as a means for communication between two processes, read-only shared memory can be used as a means of memory optimization. In case of shared libraries this does not only reduce the memory footprint of a system but also enhances the speed as shared code is kept only once in memory and in CPU caches as well as address translation units. The operating system implements this behavior by mapping the same physical memory into the address space of each process.

When executing self-modifying code or just-in-time compiled code, this advantage cannot be used in general. Android applications are usually implemented in Java and therefore would incur just-in-time compilation. However, there have been several approaches to improve the performance, first with optimized virtual machine binaries and more recently with native code binaries that are compiled from Java byte code using ART (Android Runtime).

The operating system employs the same memory sharing mechanism when opening a file as read-only and mapping it into memory using system calls like `mmap` . Thus, an attacker can map code or data of a shared library or any accessible binary into its own address space, resulting in read-only shared memory, even if the program is statically linked.

Content-based page deduplication is another form of shared memory. Here, an operating system service scans the entire system memory for identical physical pages. Identical pages are merged to the same physical page and marked as copy-on-write. This mechanism can enhance system performance in cases where system memory is scarce, such as cloud systems with a high number of virtual machines or smartphones with limited physical memory.

Processes can retrieve information on virtual and physical address mappings using operating-system services like `/proc/<pid>/maps` or `/proc/<pid>/pagemap`, both on Linux and on Android. While Linux gradually restricts unprivileged access to these resources, these patches have not yet been merged into stock Android kernels. Thus, a process can retrieve a list of all loaded shared-object files and the program binary of any process and even perform virtual to physical address translation without any privileges.

### C. Cache Attacks

In the groundbreaking work of Kocher \cite{50} about timing attacks on cryptographic implementations, the CPU cache has been first mentioned as possible information leak. Later, Kelsey et al. \cite{28} observed that cache-hit ratios can be exploited in order to break ciphers employing large S-boxes. Based on these theoretical observations, more practical attacks against DES have been proposed by Page \cite{43} and also by Tsunoo et al. \cite{54}. With the standardization of the Advanced Encryption Standard (AES) \cite{14}, \cite{57}, cache attacks against this block cipher have been investigated, i.e., Bernstein \cite{8} presented the well-known cache-timing attack against AES that has been further analyzed by Neve \cite{38} and Neve et al. \cite{40}.

While Bernstein’s cache-timing attack exploited the overall execution time of the encryption algorithm, more fine-grained exploitations of the memory accesses to the CPU cache have been proposed by Percival \cite{44} and also by Osvik et al. \cite{42}. More specifically, Osvik et al. formalized two concepts, namely Evict+Time and Prime+Probe, to determine which specific cache sets have been accessed by a victim program. Both of these approaches consist of three basic steps which are outlined within the following paragraphs.

#### Evict+Time:
1) Measure the execution time of the victim program.
2) Evict a specific cache set.
3) Measure the execution time of the victim program again.

#### Prime+Probe:
1) Occupy specific cache sets.
2) The victim program is scheduled.
3) Determine which cache sets are still occupied.

Both approaches, Evict+Time and Prime+Probe, allow an adversary to determine which cache sets are used during the victim’s computations and have been exploited to attack cryptographic implementations (cf. \cite{23}, \cite{32}, \cite{42}, \cite{53}) but also to build cross-VM covert channels (cf. \cite{35}).

A significantly more powerful, i.e., more fine-grained, attack approach denoted as Flush+Reload has been proposed by Yarom and Falkner \cite{58} in 2014. This sophisticated technique exploits three fundamental concepts of modern system architectures. First, the availability of shared memory between the victim process and the adversary. Second, last-level caches...
are typically shared among all cores. Third, Intel platforms use inclusive last-level caches, meaning that the eviction of information from the last-level cache leads to the eviction of this data from all lower-level caches of other cores, which allows any program to evict data from other programs on other cores. While the basic idea of this attack has been proposed by Gullasch et al. [20], Yarom and Falkner extended this idea to shared last-level caches which allows for cross-core attacks. The basic working principle of Flush+Reload is as follows.

**Flush+Reload:**

1) Map binary (shared object or program) into address space.
2) Flush a specific cache line (code or data) from the cache.
3) Schedule the victim program.
4) Check if the corresponding code from step 2) has been loaded by the victim program.

Thereby, the Flush+Reload approach allows an attacker to determine which specific instructions are executed and also which specific data is accessed by the victim program. Thus, rather fine-grained attacks are possible and have already been demonstrated against cryptographic implementations (cf. [21], [25], [26]). Furthermore, Gruss et al. [18] demonstrated the possibility to automatically exploit cache-based side-channel information based on the Flush+Reload approach. Besides attacking cryptographic implementations like AES T-table implementations, they showed how to infer keystroke information and even how to build a keylogger according to the cache side channel. Similarly, Oren et al. [41] demonstrated the possibility to exploit cache attacks on Intel platforms from JavaScript and showed how to infer visited websites and to track the user’s mouse activity.

While the above discussed attacks have been proposed and investigated for Intel processors, only few studies consider the possible exploitation of cache-based side-channel information on modern smartphones. So far, these investigations on modern smartphone platforms, like ARM Cortex-A processors, only considered the exploitation of cache attacks in order to attack cryptographic implementations. For instance, Weiß et al. [56] investigated Bernstein’s cache-timing attack on a Beagleboard employing an ARM Cortex-A8 processor. As Weiß et al. claimed that noise makes the attack difficult, Spreitzer and Plös [51] investigated the applicability of Bernstein’s cache-timing attack on different ARM Cortex-A8 and ARM Cortex-A9 smartphones running the Android operating system. Both investigations [51], [56] confirmed that timing information is leaking, but two major drawbacks restrict the practical application of this attack. First, many measurement samples are required, e.g., about 2^{30} AES encryptions, and second, the key space could only be reduced to about 65 bits which is still rather impractical. Later on, Spreitzer and Gérard [49] improved upon these results and managed to reduce the key space to a complexity which is practically relevant.

Besides Bernstein’s cache-timing attack, another attack against AES T-table implementations has been proposed by Bogdanov et al. [9], who exploited so-called wide collisions on an ARM9 microprocessor. In addition, power analysis attacks [16] and also electromagnetic emanations [15] have been shown to be powerful techniques to visualize cache accesses during AES computations on ARM microprocessors. Furthermore, Spreitzer and Plos [50] implemented the Evict+Time approach in order to attack an AES T-table implementation on Android-based smartphones. However, so far only cache attacks against the AES T-table implementation have been considered on smartphone platforms and none of the most recent advances has been evaluated and investigated on mobile devices. As mobile devices advance to be the major computing platforms, we consider it especially important to further investigate the possible threat arising from cache attacks. In this paper, we aim to close this gap.

### III. Adversary Model and Attack Scenario

As we consider a scenario where an adversary attacks a smartphone user, we obviously require the user to install a malicious application. Nevertheless, we consider this a realistic assumption due to the following reasons.

1) **Non-rooted smartphones**: Our application does not require a rooted smartphone as the malicious application can be executed in unprivileged userspace.
2) **No permissions**: Our application does not require any permission at all, which means that users will not be able to notice any suspicious behavior due to the presented permissions during the install process.
3) **Malicious app can be spread through popular app markets**: Based on the above mentioned advantages, we note that such a malicious application can be spread easily via available app markets, such as Google Play and the Amazon Appstore. An adversary only needs to convince the user to install our application, which can be done through a useful tool or an addictive game.
4) **Independent of Android version**: Our presented attack does not rely on a specific Android version and works on all stock Android ROMs as well as customized ROMs in use today.

We derive the prerequisites for our Evict+Reload attack according to the challenges identified in Section [I].

1) **Efficient eviction without a dedicated flush instruction**: On ARM platforms we are facing two obstacles that need to be overcome. First, the dedicated flush instruction is restricted to privileged mode only. As our attack should be deployable without any privileged instructions, i.e., on non-rooted devices, we need to rely on memory accesses to congruent addresses in order to evict data from the cache. Second, due to the random replacement policy current attacks on ARM platforms [50] rely on a number of memory accesses which is two to three times the number of ways. Thus, we optimize the number of memory accesses, i.e., a more efficient cache eviction.
2) **Precise timings without performance monitor registers**: Cache attacks on ARM use the PMCCNTR register [3], which allows for cycle-accurate timing measurements. However, access to this register must be granted by a privileged application, which means that a rooted smartphone is required for state-of-the-art cache attacks. Even though the challenge of launching cache attacks on non-rooted devices has been mentioned by Spreitzer and Plos [50] as interesting future work, it has not been solved yet.
3) **Shared memory between applications**: The Flush+Reload attack proposed by Yarom and Falkner [58] requires read-only shared memory between a spy process and a...
victim process. This ensures that both processes work on the same physical addresses and the spy process can determine the victim’s memory accesses by means of cache hits and cache misses, respectively.

4) Shared inclusive/exclusive last-level cache: The Flush+Reload attack also relies on a shared inclusive last-level cache. The most recent ARM Cortex-A53/A57 generation has a unified shared last-level cache that is inclusive on the instruction side and exclusive on the data side. We investigate how this cache can be instrumented to implement Flush+Reload-like attacks. In addition, we show how to launch our presented attack even against shared last-level caches that are neither inclusive nor exclusive and, thus, our attack can be used to attack older ARM Cortex-A8 and ARM Cortex-A9 devices as well.

The same prerequisites also apply for the Prime+Probe attack, except that the spy and the victim process do not need to share memory.

Within the next Section we show how to fulfill all these prerequisites and how an adversary can exploit these features in order to launch generic cache template attacks as described by Gruss et al. [18].

IV. THE EVICT+RELOAD ATTACK

In this section we present Evict+Reload, a highly accurate access-based cross-core cache side-channel attack. It is a variant of the Flush+Reload attack proposed by Yarom and Falkner [58] and has been first mentioned by Gruss et al. [18] as an alternative to Flush+Reload. Instead of using an instruction to flush data from the cache, Evict+Reload evicts data from the cache by performing memory accesses, similarly as in Evict+Time or Prime+Probe attacks. However, Gruss et al. observed that Evict+Reload has no practical use on x86 platforms as the clflush instruction is available in unprivileged mode on Intel platforms. While the ARMv7-A and the ARMv8-A instruction sets support various privileged flush instructions, there is no flush instruction that is accessible from userspace [3]. Thus, we need to rely on memory accesses for eviction purposes.

The Evict+Reload attack as described by Gruss et al. is specifically tailored to the x86 architecture and assumes the availability of several x86 instructions, such as rdtsc. Therefore, it is not directly applicable to ARMv7-A and ARMv8-A architectures. We first describe Evict+Reload in a generic way and subsequently we show how it can be implemented on ARMv7-based architectures.

Similarly to the Flush+Reload attack, Evict+Reload relies on the availability of shared memory between the attacker and the victim, e.g., shared libraries or program binaries. Following the notion of Flush+Reload, the attacker process maps the library or binary under attack into its own virtual address space. The attacker then “probes” addresses within this shared memory area. More specifically, for each address $a$ within the shared memory area, the attacker evicts address $a$ from the CPU cache, waits for the victim process to be scheduled, and finally the attacker determines whether the victim fetched address $a$ into the CPU cache again. Algorithm 1 summarizes the single steps for a specific address $a$.

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Algorithm 1: Evict+Reload attack

| Input: Address $a$ of mapped shared memory $m$ |
| Output: Cache hit/miss on address $a$ after victim has been scheduled |

Evict address $a$ from cache
Wait for victim to be scheduled
Check whether or not victim loaded $a$ into the cache

if Victim loaded $a$ into the cache then
  | return Hit |
else
  | return Miss |
end

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The basic idea is that depending on whether or not the victim process accessed the memory region (instruction or data) corresponding to address $a$, the attacker either observes a cache hit or a cache miss when addressing address $a$ again. Therefore, either timing information, a cycle counter, an instruction counter, or a cache-miss counter can be employed. In case the attacker observes a cache hit, the victim process must have loaded the memory address $a$ into the cache before. Otherwise, the attacker learns that the victim most likely did not access this address. The Evict+Reload attack has a high accuracy as it is highly unlikely that exactly one cache line is evicted by other system activity before the attacker is able to reload it. However, if the victim’s access happens after the reload step and before finishing eviction in the next iteration, the cache line can be evicted by the attacker accidentally. The execution time of this code fragment is always below 1 μs. By choosing the duration of the waiting step, the attacker chooses a trade-off between the temporal resolution and the probability of missing an event. For instance, a waiting duration of 1 ms yields a probability below 0.1% to miss an event while still being accurate enough for most use cases. In other scenarios, spy and victim might be synchronized as the spy triggers the victim computation. In this case the probability of missing a cache hit is even lower.

As already mentioned above, an attacker can rely on various mechanisms, e.g., timing information or a performance counter like a cache-miss counter, in order to distinguish between cache hits and cache misses. In this work we employ a cycle-accurate timer in order to distinguish between a cache hit and cache miss. Figure 1 illustrates a histogram for memory accesses resulting in a cache hit and memory accesses resulting in a cache miss. Based on this histogram, an attacker can reliably determine a threshold to distinguish between cache hits and cache misses, which is then used in Algorithm 1. The plot in Figure 1 is based on the privileged cycle counter register (PMCCNTR). However, we will demonstrate a means to overcome this privileged register in Section IV-B.

As already mentioned in Section III, a few challenges need to be overcome in order for Evict+Reload to be applicable for our adversary model. Within the following subsections we investigate how to fulfill all the requirements for our attack strategy. First, we discuss the technicalities in order for our attack to work on shared inclusive as well as shared exclusive last-level caches. Afterwards, we show how to get rid of the prerequisite of a rooted smartphone in order to get cycle-accurate timings. Last but not least, we show how to evict
specific cache sets without relying on the privileged flush instruction.

A. Shared Cache Lines on ARM CPUs

Sharing memory between victim and spy process is straightforward on Linux and Windows. As the operating system tries to minimize the memory footprint, binaries and shared objects are always mapped as read-only shared memory into all processes. Since Android is based on Linux, the same concepts also apply to the Android OS. Even though most Android applications are implemented in Java and, thus, sharing memory between a spy and a victim process is more difficult, the underlying system employs shared memory just as in Linux. Hence, we target shared libraries or program binaries on Android as well.

When it comes to caches, ARMv7-A and ARMv8-A CPUs are very heterogeneous compared to Intel CPUs. Whether a CPU has a second-level cache can be decided by the manufacturer. As we only consider multi-core CPUs with a second-level cache as they are predominant in Android smartphones, there is only a limited number of properties that influence whether cache lines are shared and to what extent. The last-level cache on ARMv7-A and ARMv8-A devices is usually shared among all cores. However, the last-level cache can be inclusive to lower-level caches, that is every cache line in any core’s lower-level cache is also contained in the last-level cache. It can also be exclusive, that is no cache line can be in both cache levels at the same time. ARMv7-A CPUs, i.e., ARM Cortex-A8 and ARM Cortex-A9 processors, are usually neither inclusive nor exclusive. Thus it is difficult to perform cross-core attacks. However, in this scenario an attacker can run the spy process on all cores simultaneously and thus fall back to a same-core attack. This changed with the ARMv8-A architecture, e.g., ARM Cortex-A53 and ARM Cortex-A57 processors. On this architecture the last-level cache is inclusive on the instruction side and exclusive on the data side [1], [5].

To perform a cross-core attack we do not execute the instructions we want to spy on. Instead we load enough data into the cache to fully evict the corresponding last-level cache set. Thereby, we exploit that the last-level cache is inclusive on the instruction cache side and can evict instructions from the other core’s local caches. Figure 2 illustrates such an eviction. In step 1, an allocation is made to the last-level cache and the instruction cache of one core. In step 2, a process fills its core’s data cache, thereby evicting cache lines into the last-level cache. In step 3, the process has filled the last-level cache set using only data accesses and thereby evicts the instructions from other core’s instruction caches as well.

Although the data caches are exclusive, we observe that we can perform cross-core attacks on these caches as well. After evicting data from the last-level cache using memory accesses we measure higher access times. When another process running on a different core reaccesses the data we observe a lower access time again. These timing measurements would suggest an inclusive cache architecture although it is exclusive according to the documentation [1], [5]. We assume that this is due to the cache-coherency protocol between the CPU cores. If remote-core data fetches are performed instead of accesses to physical memory it might be fast enough to be observed as a cache hit. However, this attack is generally not possible on exclusive last-level caches. Further investigations on exclusive last-level caches and the influence of cache-coherency protocols are beyond the scope of this work and we consider these investigations as possible future work.

On the Krait 400 the L2 cache is neither inclusive on the data side nor on the instruction side. However, we observed that cross-core cache attacks are still possible in most cases. The reason for this could be the cache-coherency protocol between the CPU cores. In cases where the Evict+Reload attack did not work on the Krait 400 we found that launching the attack in parallel on all CPU cores allows to perform Evict+Reload in a local-core attack. Thus, the attack can be applied to older devices with non-inclusive caches as well.

B. Distinguishing Cache Hits and Cache Misses

In order to distinguish cache hits and cache misses, timing sources or dedicated performance counters can be used, i.e., anything that captures the difference between cache hits and cache misses. We focus on timing sources as cache misses have a significantly higher access latency. While cache attacks on x86 CPUs employ the rdtsc instruction—which provides sub-nanosecond resolution timestamps—that can be accessed by any unprivileged user program, the ARMv7-A architecture does not provide an instruction for this purpose. Instead, the ARMv7-A architecture has a performance monitoring unit that allows to monitor CPU activity. One of these performance counters—denoted as cycle count register (PMCCNTR)—can be used to distinguish between a cache hit and a cache miss by relying on the number of CPU cycles that passed during a memory access. However, the performance monitoring unit is not accessible from userspace by default.
Previous work assumed that an attacker is able to enable userspace access to these performance counters by setting a certain register while running in privileged mode. In order to do so, it is required to obtain root privileges on the device and to load a kernel module. While this is possible on rooted devices if specific applications are installed and executed, the vast majority of Android smartphones are not rooted.

Thus, in order to broaden the attack surface, we do not want to rely on root privileges in order for our attack to work. Our observations showed that in Linux kernel version 2.6.31 the `perf_event_open` syscall has been introduced as an abstract layer to access runtime performance information independent of the underlying hardware. It allows to access performance counters on different CPUs through a unified interface. In our case we use the `PERF_COUNT_HW_CPU_CYCLES` performance counter that returns an accurate cycle count just as the privileged instructions. However, due to the fact that this approach relies on a syscall to acquire the cycle counter value, a latency overhead can be observed.

In Figure 3 we show the cycle count distribution as measured using the `perf_event_open` interface and via access to the privileged PMCCNTR register. Although the system call introduces latency and noise, cache hits and cache misses are still clearly distinguishable. Thus, even with this latency overhead we are able to exploit this syscall in order to successfully launch our proposed Evict+Reload attack.

Through this syscall interface, it is possible to get the CPU cycle counter value from userspace without privileged access. Since only Android 1.0 used a kernel version below 2.6.31 and more recent Android versions deploy kernel versions 3.4 or 3.10, the `perf_event_open` interface is available on all Android devices above Android 1.0. Furthermore, today the number of devices running Android 1.0 is negligible and, therefore, we assume that about 1.4 billion Android devices [33] are affected.

C. Unprivileged Cache Eviction

As described in Section II-A, modern CPUs employ set-associative caches. Multiple cache lines comprise one cache set and addresses that map into the same set are considered as congruent. These congruent addresses compete for cache lines in this set. If a cache line has to be allocated for data fetched from the physical memory, an existing cache line needs to be replaced, i.e., evicted according to a predefined replacement policy. The ARMv7-A architecture defines two different cache replacement policies, namely round-robin and pseudo-random replacement policy. In practice only the pseudo-random replacement policy is used for reasons of performance and since switching the cache replacement policy is only possible in privileged mode.

In order to intentionally evict a specific cache set without a dedicated flush instruction, an attacker needs to access congruent memory addresses that map to the same cache set. This has already been proposed by Osvik et al. [42]. Similarly, Hund et al. [22] flush the whole CPU cache on an older Intel CPU without using cache maintenance operations by accessing a physically consecutive memory buffer which is larger than the cache. Although this also evicts the targeted address it is definitely not the fastest approach, as it would be sufficient to access only addresses which are congruent to the address to be evicted. Cache eviction has recently been investigated in more detail for the x86 architecture [32], [35], [41] in order to perform Prime+Probe attacks. However, as already observed by Spreitzer and Plos [50], on ARMv7-A CPUs it is necessary to access more addresses than there are cache lines per cache set, because of the pseudo-random replacement policy. We improve these eviction strategies by applying methods of Gruss et al. [17].

While the cache replacement on ARM Cortex-A processors is described as a pseudo-random replacement policy, there are no details on the actual implementation. Gruss et al. [17] recently proposed an algorithm to find access patterns that achieve a high eviction rate and a low execution time on Intel CPUs. Although they claim that their algorithm works on any architecture, they only examined different Intel architectures. While their algorithm is very slow and computes both, congruent addresses and an access pattern, we only need to search for the access pattern. This is due to the fact that Android provides access to the mapping of virtual to physical addresses through `/proc/self/pagemap`. Although access to this mapping has already been identified as a potential security issue on x86 [47] and recent Linux kernels [29] restrict access to this mapping, current Android versions still allow access to any unprivileged application. Therefore, we can compute congruent addresses directly and only use their algorithm to evaluate the access patterns using our set of congruent addresses.

We applied the algorithm of Gruss et al. [17] to the set of congruent addresses—which has been established via the access to `/proc/pid/pagemap`—for our two test devices. Figure 4 shows the best access pattern for the Krait 400 CPU. On the y-axis we illustrate the different (but congruent) addresses and on the x-axis we illustrate the memory accesses over time. Hence, for the Krait 400, which has a 4-way L1 cache and an 8-way L2 cache, our eviction set consists of a total of 12 congruent addresses. These addresses are accessed using read accesses within a loop of 10 rounds, with 3 memory accesses per round, and these accesses are shifted by 1 after every round. Based on this eviction strategy, we measured an eviction rate of 100% and an average execution time of 599 cycles if performed in an Evict+Reload attack. Although a strategy accessing every address in the eviction set only once would perform significantly less memory accesses, it consumes...
more CPU cycles. For an eviction rate of 100\% the eviction set size is at least 16 and the execution time at least 1460 cycles in the same attack scenario.

Table I summarizes different eviction strategies for the Krait 400. The first column indicates the total eviction set size \(N\). \(A\) denotes the shift offset to be applied after each round and \(D\) indicates the number of memory accesses in each iteration. The column \(cycles\) states the execution time for the eviction and the last column indicates the eviction rate. For instance, a strategy with the same loop as before, but only 2 accesses to different addresses per round over 13 rounds has an average execution time of only 582 cycles but the eviction rate drops to 50\%. The first line in Table I states the execution time and the eviction rate for the privileged flush instruction, which gives the best result in terms of execution time (549 cycles). Our best identified eviction strategy also achieves an eviction rate of 100\% but takes 599 cycles. Thus, there is a small trade-off between using the optimal but privileged flush instruction and the unprivileged eviction strategy which takes slightly more time.

We performed the same evaluation on our ARM Cortex-A53 test system. Figure 4 shows an excerpt of the best eviction pattern we found for this CPU. The access pattern consists of a loop of 18 rounds, each with 4 repeated memory accesses to the same 6 addresses and where these accesses are shifted by 1 in each iteration. Thus the eviction set contains 23 different addresses for the ARM Cortex-A53 with a 4-way L1 cache and a 16-way L2 cache. Based on this eviction strategy, we measured an eviction rate of 99.86\% and an average execution time of 8789 cycles. Again accessing every address only once in the eviction set only once is much less efficient although it involves significantly less memory accesses. For this strategy, we had to increase the eviction set size to 800 to achieve an eviction rate of 99.04\%. Eviction then takes 131804 cycles, which is 15 times as much as with the best strategy we found. We suspect the reason for this in exclusiveness of the L2 cache on the data side. We can only fill an L2 cache set by evicting the corresponding address in the shared library. To transmit a bit value of 1, the sender accesses the corresponding address in the shared library that is used by both, the sender and the receiver. While both processes have read-only access to the shared library, they can transmit information by loading addresses from the shared library into the cache or evicting it from the cache.

We implement the covert channel using a simple protocol. Data is transmitted in \(n\) bits, an additional \(s\)-bit sequence number, and a \(c\)-bit checksum that is calculated over the payload and the sequence number. The sequence number is used to distinguish consecutive packages and the checksum is used to check the integrity of the payload and the sequence number. If a received data package is valid, the \(s\)-bit sequence number is sent back accompanied with an additional \(x\)-bit checksum calculated over the returned sequence number. By adjusting the sizes of checksums and sequence numbers the error rate of the covert channel can be controlled. Figure 6 illustrates the data frames for sending data and the corresponding responses.

Each bit is represented by one address in the shared library, while no two addresses are chosen that map to the same cache set. In order to transmit a bit value of 1, the sender accesses the corresponding address in the shared library. To transmit a bit value of 0, the sender does not access the corresponding address, resulting in a cache miss on the receiver’s side. Thus, the receiving process observes a cache hit or a cache miss depending on the memory access performed by the sender. The sender then checks whether the acknowledge bit has been set by the receiver. If it is set, the response sequence number will be measured on the corresponding cache sets. If the response

![Fig. 4. Optimal access pattern on our Krait 400 test device.](image)

![Fig. 5. Excerpt of the optimal access pattern on our Cortex-A53 test device.](image)

![Fig. 6. Format of send data frames (above) and response data frames (below).](image)

Table I. Different eviction strategies on the Krait 400

<table>
<thead>
<tr>
<th>(N)</th>
<th>(A)</th>
<th>(D)</th>
<th>Cycles</th>
<th>Rate</th>
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<td>3</td>
<td>2</td>
<td>32</td>
<td>0.00%</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>3</td>
<td>599</td>
<td>100.00%</td>
</tr>
<tr>
<td>13</td>
<td>1</td>
<td>2</td>
<td>582</td>
<td>50.03%</td>
</tr>
<tr>
<td>32</td>
<td>3</td>
<td>2</td>
<td>16689</td>
<td>99.97%</td>
</tr>
</tbody>
</table>

V. A HIGH PERFORMANCE CACHE COVERT CHANNEL

In this Section we describe a high performance cross-core cache covert channel on modern smartphones using Evict+Reload. A covert channel enables two unprivileged applications on a system to communicate with each other without using any data transfer mechanisms provided by the operating system. This communication evades the sandboxing concept and the permission system. Particularly on Android this is a problem, as this covert channel can be used to exfiltrate private data from the device that the Android permission system would normally restrict. An attacker could use one application that has access to the personal contacts of the owner of the device to send data via the covert channel to another application that has Internet access (cf. collusion attacks [34]). In such a scenario an adversary can steal personal information.

Our covert channel is established on addresses of a shared library that is used by both, the sender and the receiver. While both processes have read-only access to the shared library, they can transmit information by loading addresses from the shared library into the cache or evicting it from the cache.

We perform the same evaluation on our ARM Cortex-A53 test system. Figure 4 shows an excerpt of the best eviction pattern we found for this CPU. The access pattern consists of a loop of 18 rounds, each with 4 repeated memory accesses to the same 6 addresses and where these accesses are shifted by 1 in each iteration. Thus the eviction set contains 23 different addresses for the ARM Cortex-A53 with a 4-way L1 cache and a 16-way L2 cache. Based on this eviction strategy, we measured an eviction rate of 99.86\% and an average execution time of 8789 cycles. Again accessing every address only once in the eviction set only once is much less efficient although it involves significantly less memory accesses. For this strategy, we had to increase the eviction set size to 800 to achieve an eviction rate of 99.04\%. Eviction then takes 131804 cycles, which is 15 times as much as with the best strategy we found. We suspect the reason for this in exclusiveness of the L2 cache on the data side. We can only fill an L2 cache set by evicting the data that is already in the L2 cache and gradually add new addresses to the set instead of accessing more different addresses.
sequence number and the response checksum are valid, the sender continues with the next packet and resends the current packet otherwise. Algorithm 2 and Algorithm 3 provide a more formal description of the sender and the receiver, respectively.

**Algorithm 2: Sending data**
```
Input: Mapped shared library m
Input: Data to send d
sn ← Initial sequence number;
for fn ← 1 to number of frames do
    p ← Current package (sn, d, CS(fn, d_x));
    received ← false;
    do
        Access sending bit address;
        Access or evict packet bit addresses;
        ack ← Access Acknowledge bit address;
        if ack ≡ true then
            Measure response data addresses;
            sn_m, cs_m ← Response seq. number, CRC;
            if CS(sn, d) ≡ cs_m and sn ≡ sn_m then
                received ← true;
            end
        end
    while received ≡ false;
    sn ← sn + 1;
end
```

**Algorithm 3: Receiving data**
```
Input: Mapped shared library m
while true do
    received ← false;
    do
        sn ← Initial sequence number;
        sending ← false;
        do
            sending ← Measure sending bit address;
            while sending ≡ false;
            Measure packet data addresses;
            sn_m, cs_m ← Sequence number, data, CRC;
            if CS(sn_m, d_m) ≡ cs_m then
                if sn ≡ sn_m then
                    received ← true;
                    Report d_m;
                    sn ← sn + 1;
                end
            end
            Access acknowledge bit address;
            Access or evict response data bit addresses;
        else
            Evict acknowledge bit address;
        end
    while received ≡ false;
end
```

We implemented this covert channel on our ARM Cortex-A53 device with the following parameters. We use an 8-bit checksum, a 64-bit payload, and an 8-bit sequence number. According to these parameters, we achieve a transmission rate of 18.534 bps. A practical evaluation of our implementation of the proposed covert channel with these parameters yields an error rate of 0%, which indicates that further improvements might be possible. In particular the packet payload size can be increased or checksum and sequence number size decreased until the error rate reaches 1% while increasing the overall transmission rate. However, the comparison in Table II shows that our covert channel clearly outperforms existing covert channels by a factor of 4 in terms of bandwidth. In addition, Marforio et al. [34] also reported that the XManDroid framework [10][11] is able to detect the Type of Intents covert channel as well as the UNIX socket discovery channel, which indicates that the previously fastest covert channels can already be prevented.

### VI. Side-Channel Attacks on Mobile Devices

In this section we demonstrate access-driven cache-sidechannel attacks on mobile Android devices. We implement cache template attacks as described by Gruss et al. [18] to create and exploit accurate cache-usage profiles using the **Evict+Reload** attack. Cache template attacks consist of a profiling phase and an exploitation phase. In the profiling phase, a template matrix is computed that represents how many cache hits occur on a specific address after triggering a specific event. The exploitation phase uses this matrix to infer events from cache hits. For further details about cache template attacks we refer to Gruss et al. [18].

To perform cache template attacks, an attacker has to be able map shared binaries or shared libraries as read-only shared memory into its own address space. We have already shown that this is possible in the previous section. By using shared libraries, the attacker bypasses any potential countermeasures taken by the operating system, such as restricted access to runtime data of other apps or address space layout randomization (ASLR). The attack can even be performed online on the device under attack if the event can be simulated. We exemplary show how to simulate these events in case of touch actions below.

Within the following subsections we show how cache template attacks can be used to infer touch actions and keystrokes on Android-based smartphones. Furthermore, we demonstrate an effective attack against the AES T-table implementation, which is still deployed on all smartphones running stock versions of Android.

#### A. Inferring Touch Actions and Keystrokes

We launched cache template attacks on user input events in order to find addresses in shared libraries that are responsible for user input handling. After identifying such addresses, the idea of cache template attacks is to monitor these addresses in order to infer user input events. Just as Linux, Android uses a large number of shared libraries, each with a size of up to several megabytes. We inspected all available libraries on the

<table>
<thead>
<tr>
<th>Work</th>
<th>Type</th>
<th>Permission</th>
<th>Bandwidth [bps]</th>
</tr>
</thead>
<tbody>
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<td>Ours</td>
<td>Cache</td>
<td>-</td>
<td>18 534</td>
</tr>
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<td>Marforio et al. [34]</td>
<td>Type of Intents</td>
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<td>4 300</td>
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<td>-</td>
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<td>Schlegel et al. [35]</td>
<td>Screen wake lock</td>
<td>WAKE_LOCK</td>
<td>5</td>
</tr>
</tbody>
</table>
system by manually scanning the names and identified libraries that might be responsible for handling user input, e.g., like the libinput.so library.

After we identified libinput.so as our main target library, we launched the profiling phase of the cache template attack. Thus, we simulated the user input events like tapping or swiping on the screen as well as sending text and key events to applications. We simulated these events via the android-debug bridge (adb shell) with two different methods:

The first method uses the input command line tool to simulate user input events. The second method is writing event messages to /dev/input/event*. As the second method only requires a write() statement it is significantly faster, but it is also more device specific. Therefore, we used the input command line tool in most scenarios. While simulating these events, we simultaneously probed all addresses within the libinput.so library, i.e., we measured the number of cache hits that occurred on each address after triggering a specific event.

Figure 7 shows the cache template matrix for the libinput.so library. We triggered the following events: key events including the power button (key), long touch events (longpress), swipe events, touch events (tap), and text input events (text) via the input command line tool as often as possible and measured each address for one second. The cache template matrix clearly reveals addresses with high cache-hit rates for the corresponding events. More specifically, squares with a darker color represent addresses with a higher cache-hit rate for the corresponding event, whereas lighter colors represent addresses with lower cache-hit rates. Hence, the cache template matrix reveals addresses that can be used to distinguish different events.

We also verified the previously revealed addresses by monitoring the identified addresses while operating the smartphone manually, i.e., we touched the screen and our t

darken template matrix to infer the events does neither require privileged access nor any permission.

Fig. 7. Cache template matrix for libinput.so.

tack application reliably reported cache hits on the monitored addresses. For instance, on address 0x11040 of /system/lib/libinput.so on our ARM Cortex-A53 test device.
shown by Zhang et al. [59]. Furthermore, even though our evaluations so far did not reveal any addresses that leak entered keys directly, we can distinguish between keystrokes on the soft-keyboard and generic touch actions outside the soft-keyboard. This information can be used to enhance existing sensor-based keyloggers. Sensor-based keyloggers exploit sensors in mobile devices in order to infer the users’ input on these devices. Examples include, for instance, the exploitation of the accelerometer and the gyroscope [6], [12], [13], [36], [57], and also the ambient-light sensor [48]. However, many of these attacks suffer from a lack of knowledge when exactly a user touches the screen. Based on our attack, an attacker can improve upon these sensor-based keyloggers as our attack allows to infer (1) the exact time when the user touches the screen, and (2) whether the user touches the soft-keyboard or any other region of the display.

B. Attack on Mobile AES Implementations

Cache attacks against AES T-table implementations have already been demonstrated extensively. Eventually, countermeasures against these types of attacks have already been proposed in order to prevent these attacks against AES. Among these countermeasures are, for instance, so-called bitsliced implementations [27], [31], [45]. Furthermore, Intel addressed the problem by adding dedicated instructions for AES [19], and also ARM follows the same direction with the ARMv8 instruction set [4]. Thus, the academic community seems to agree that attacking AES T-table implementations has become irrelevant. However, our investigations showed that the OpenSSL library as well as the Bouncy Castle crypto implementation on Android devices still use the T-table implementation, which might be due to performance reasons. These T-tables contain the precomputed round transformations \( \text{SubBytes} \), \( \text{ShiftRows} \), and \( \text{MixColumns} \). The most-widely employed implementation uses five T-tables \( T_i \), whereas \( T_0 \) to \( T_3 \) are used during the first 9 rounds, and the last round uses \( T_4 \) due to the fact that the last round omits the \( \text{MixColumns} \) transformation. However, variants of this implementation with fewer tables also exist. The appealing benefit of T-table implementations is that encryption and decryption operations can be computed by simple XOR operations. For instance, let \( p_i \) denote the plaintext byte, \( k_i \) the initial key byte, and \( s_i = p_i \oplus k_i \) the initial state after the first \( \text{AddRoundKey} \) transformation. The initial state is then used to retrieve the precomputed elements via \( T_j[s_i] \), where \( i \equiv j \mod 16 \), which are then used to form the state for the next round.

Now, if an attacker knows the plaintext as well as the corresponding entries of the T-table that have been accessed, parts of the key bytes can be recovered via \( k_i = s_i \oplus p_i \).
For further details about this attack we refer to the work of Osvik et al. [42], [53]. For the sake of simplicity—and since we only want to compare our results with related work—we consider a first-round attack only. However, more sophisticated attacks considering the first two rounds and also attacks considering the last round also exist [39], [53].

Stock Android versions ship OpenSSL 1.0.1 or earlier. This version provides an optimized AES implementation for ARM using a single 1KB S-Box. If certain flags during compile time are not set it will fall back to the default vulnerable T-table implementation of AES. We have successfully performed a template attack on such an OpenSSL library using AES with T-tables to show that our attack works. The first round attack requires as little as 224 encryptions per key byte to reduce the key space to 64 bits. Similarly, the OpenSSL library shipped with stock Android versions could be attacked by means of a last-round attack. However, to perform a more realistic attack we need to attack an implementation that is widely used in practice.

In order to do so, we focus on the Bouncy Castle AES implementation, which is the default cryptographic provider for Android apps. Bouncy Castle is implemented in Java and uses an AES T-table implementation by default, although T-table implementations are known to be vulnerable against side-channel attacks. Our attack of Bouncy Castle therefore affects up to 1.4 billion Android users. Furthermore, we are the first to show that even Java implementations can be attacked.

When the Bouncy Castle library is initialized in an Android application, copies of the T-tables are created. These copies are local and therefore not shared among multiple processes. Thus an Evict+Reload attack would only be possible within the same process but not in any real-world attack. However, to investigate the Evict+Reload attack and whether the Bouncy Castle library is generally susceptible to cache side-channel attacks we perform an attack within the same process using the Evict+Reload attack. Figure 11 shows a template matrix of the first T-table for all 256 values for key byte \( k_0 \) and a fixed plaintext 0 while the remaining key bytes are random.

We can see that the correct value of the upper 4 bits of the key byte can clearly be determined from the observed cache hits (cf. [42], [50]). The first round attack requires only 512 encryptions per key byte to reduce the key space to 64 bits. However, we also see that the T-table is not aligned. We found that the T-tables are placed on a different boundary every time the process is started. If it is possible to trigger a restart of the victim application, it is possible to find an arbitrary disalignment.

As shown by Spreitzer and Plos [50], disaligned T-tables leak additional information as a smaller set of look-up indices \( s_i = k_i \oplus p_i \) map to cache lines at the beginning and the end of the T-tables. They observed that on average only 20 bits of the key need to be searched exhaustively and specific disalignments even allow full-key recovery without a single brute-force computation. Later, Takahashi et al. [52] theoretically investigated this information leak. Thus, the Bouncy Castle crypto provider, which is the standard crypto provider on Android smartphones, is highly insecure.

In a real-world attack on Bouncy Castle an attacker has no access to the memory and thus is not able to perform an Evict+Reload attack on the corresponding memory region. However, a Prime+Probe attack is still possible as we describe in the next section.

VII. The Prime+Probe Attack on ARM

The eviction used in our Evict+Reload attack also enables implementing Prime+Probe attacks. While apps can access executable files of other apps and shared libraries likewise this does not mean that an attack is always possible. For instance, in case of the Bouncy Castle AES implementation, the T-tables are copied to a local memory. Therefore, the attacker has no way to share this memory region with the victim. For such scenarios we implemented Prime+Probe to perform cross-core last-level attacks without shared memory. Inherently a Prime+Probe side channel is more noisy and thus less accurate. Still it enables monitoring cache hits and misses even on dynamically generated data. The possibility of a Prime+Probe attack also shows that disabling shared memory does not prevent cache attacks on ARM.

Before performing a Prime+Probe attack, the attacker needs to identify the CPU cache sets to be attacked. In the first step of the attack, the attacker “primes”, i.e., occupies, the cache set by running the same eviction loop as in Evict+Reload. The attacker then waits for the victim to perform a computation. In the second step, the attacker “probes” the cache set by accessing all addresses from the eviction set in reverse order once again. Osvik et al. [42] have shown that the time to access the addresses in this step is directly related to the number of ways that have been replaced by the victim. If the victim replaced no ways, the “probe” step will take minimal time. If the victim replaced more ways, the “probe” step will take longer. On x86 the replacement policy facilitates this attack and an attacker can even deduce the number of ways that have been replaced in the cache set. This seems to be much more difficult on ARM, due to the random replacement policy, as has also been observed by Spreitzer and Plos [50]. However, we managed to launch a Prime+Probe attack on ARM, even though it is not as accurate as on x86 platforms. Still, we show that it can be used to spy on processes that could not be attacked otherwise. Algorithm 4 summarizes the single steps for a Prime+Probe attack on a cache set \( s \).
Our attack exploits weaknesses in hardware and in software. While building better hardware could completely prevent attacks, software weaknesses can be fixed immediately on commodity hardware and in commodity software environments. The software weaknesses we exploit exist in older as well as recent Android versions alike.

The first software weakness we exploit is the unprivileged access to the perf_event_open syscall interface. This interface allows access to an accurate cycle counter among a variety of other accurate hardware performance counters. In our attack we use this interface as a replacement to the x86 rdtsc instruction. If an attacker would not be able to retrieve an accurate cycle count it would be significantly harder to determine whether a memory access has been a cache hit or a cache miss. Therefore, we suggest making the syscall interface only available to privileged processes and especially prevent Android apps from accessing it. However, performing cache attacks without accurate timing is possible by running a second thread that increments a global variable all the time. By reading the value of the variable an attacker can retrieve a timestamp. Thus, only restricting access to the perf_event_open syscall interface is not sufficient to make the attack impossible.

The second software weakness we exploit is access to /proc/pid/pagemap information for the own process as well as other processes. In our attack we use /proc/pid/pagemap to resolve virtual addresses to physical addresses. In March 2015, Linux restricted access to /proc/pid/pagemap for other processes without elevated privileges to prevent leakage of physical addresses to unprivileged processes. Later in March access to /proc/self/pagemap has been restricted too, in order to prevent usage of virtual address resolution for Rowhammer attacks. However, the Android kernel has not yet integrated these patches. Our findings show that cache attacks in general are another reason to restrict access to /proc/pid/pagemap on all platforms. We also use /proc/pid/maps to determine shared objects mapped into the virtual address space of a victim binary. We suggest to restrict access to /proc/pid/maps such that a process can only see its own mappings and that elevated privileges are required to access information of other processes. This however, has to be fixed in the Linux kernel as well as in Android.

Third, we exploit the fact that access to shared libraries as well as dex and art optimized program binaries of other applications is only partially restricted. While we cannot re-

Algorithm 4: Prime+Probe attack

| Input: Cache set $s$ |
| Output: Time to probe cache set $s$ after victim has been scheduled |
| Prime: Occupy cache set $s$ any data |
| Wait for victim to be scheduled |
| Probe: Re-access the data from the prime step in reverse order |

if Probe time below threshold then |
return No victim access (Miss) |
else |
return Victim access (Hit) |
end

Fig. 12. Histogram of Prime+Probe probe time distribution when the victim does or does not access congruent memory as measured on the ARM Cortex-A53 test device.

As we can see in Figure 12 we can distinguish whether the victim accessed a congruent memory location. The timing is lower if the victim performed no access and higher if the victim did perform a congruent memory access. While the measurement based on Prime+Probe is significantly more noisy than in the case of Evict+Reload, it is still sufficient to perform practical attacks.

Figure 13 shows a Prime+Probe attack on the Bouncy Castle implementation of AES. For each combination of key byte and offset we performed 100 000 encryptions for illustration purposes. Although we face significantly more noise in this attack than in the Evict+Reload attack presented in the previous section, we can clearly determine the upper 4 bits per key byte using the Prime+Probe attack. The number of encryptions can even be reduced to less than 100 encryptions if the system load is low. In such a case we could reduce the key space to 64 bits within 25 600 encryptions.

VIII. COUNTERMEASURES

Our attack exploits weaknesses in hardware and in software. While building better hardware could completely prevent attacks, software weaknesses can be fixed immediately on commodity hardware and in commodity software environments. The software weaknesses we exploit exist in older as well as recent Android versions alike.

The first software weakness we exploit is the unprivileged access to the perf_event_open syscall interface. This interface allows access to an accurate cycle counter among a variety of other accurate hardware performance counters. In our attack we use this interface as a replacement to the x86 rdtsc instruction. If an attacker would not be able to retrieve an accurate cycle count it would be significantly harder to determine whether a memory access has been a cache hit or a cache miss. Therefore, we suggest making the syscall interface only available to privileged processes and especially prevent Android apps from accessing it. However, performing cache attacks without accurate timing is possible by running a second thread that increments a global variable all the time. By reading the value of the variable an attacker can retrieve a timestamp. Thus, only restricting access to the perf_event_open syscall interface is not sufficient to make the attack impossible.

The second software weakness we exploit is access to /proc/pid/pagemap information for the own process as well as other processes. In our attack we use /proc/pid/pagemap to resolve virtual addresses to physical addresses. In March 2015, Linux restricted access to /proc/pid/pagemap for other processes without elevated privileges to prevent leakage of physical addresses to unprivileged processes. Later in March access to /proc/self/pagemap has been restricted too, in order to prevent usage of virtual address resolution for Rowhammer attacks. However, the Android kernel has not yet integrated these patches. Our findings show that cache attacks in general are another reason to restrict access to /proc/pid/pagemap on all platforms. We also use /proc/pid/maps to determine shared objects mapped into the virtual address space of a victim binary. We suggest to restrict access to /proc/pid/maps such that a process can only see its own mappings and that elevated privileges are required to access information of other processes. This however, has to be fixed in the Linux kernel as well as in Android.

Third, we exploit the fact that access to shared libraries as well as dex and art optimized program binaries of other applications is only partially restricted. While we cannot re-
trieve a directory listing of /data/dalvik-cache/ all files contained are readable for any process or Android application. We propose to restrict read access to the actual owner of the file to prevent Evict+Reload attacks over these shared files.

In order to prevent cache attacks against AES T-table, a bitsliced implementation could be employed. Since OpenSSL 1.0.2 such a bitsliced implementation exists for devices capable of the ARM NEON instruction set. Furthermore, this OpenSSL version also includes supports for the ARMv8 native AES instructions. Thus, updating to this version of OpenSSL would render our attacks infeasible.

IX. Future Work

Our work shows that powerful cache attacks are also possible on recent smartphones. While this insight significantly advances the state-of-the-art in the context of cache attacks on mobile devices, we believe that this only scratches the surface of possible attacks. First, in the mobile area we have a variety in hardware and operating systems. We believe that our attack is possible on other mobile operating systems as well as long as the underlying hardware is based on the ARMv7 or ARMv8 architecture. Second, the smartphone is the most personal computing device. Existing attacks focus on stealing cryptographic keys, session tokens or spying on user input. The possibility of profiling users and spying on user activities around-the-clock shifts the focus of cache attacks to a new range of potential malicious applications. For instance, cache template attacks can be used to profile the users’ activities. The possibility of adversaries infiltrating the personal devices of millions of users emphasizes the need to investigate and implement effective countermeasures immediately.

Our attack requires the user to install a malicious app on the smartphone. However, as shown by Oren et al. [41], Prime+Probe attacks can even be performed from within browser sandboxes through remote websites using JavaScript on Intel platforms. We believe that such an attack could be implemented on smartphones as well.

Our attack on the ARM Cortex-A53 is facilitated by the introduction of the inclusiveness of the last-level cache. Removing the inclusive property to prevent cross-core cache attacks is ineffective. As we found on our Krait 400 test device, the cross-core attacks are still possible in most cases. We think that this is due to a cache-coherency protocol between CPU cores. Remote-core data fetches are most likely faster than accesses to physical memory. Thus, we might observe these remote-core data fetches as cache hits. However, this requires a cache-coherency protocol that implements this behavior. Generally, our attack is not possible on exclusive last-level caches. Although it is possible to attack these architectures by spawning one attack process per core, exclusive last-level caches should be investigated to find whether they can be attacked using cross-core cache attacks.

X. Conclusion

In this work, we proposed the first access-based cross-core cache attack on ARM-based mobile devices. Similarly to the powerful Flush+Reload attack on the x86 architecture, Evict+Reload is a highly accurate and generic cache attack. Furthermore, we show that despite the random replacement policy Prime+Probe attacks can be implemented to efficiently perform attacks in all cases where Evict+Reload is not applicable. Our work is the first to provide a comprehensive study of the Evict+Reload attack and the powerful applications of Evict+Reload and Prime+Probe on Android smartphones.

Since smartphones have become the most important personal computing devices, this work significantly broadens the scope of cache attacks. First, all cache attacks known for x86 CPUs can now be applied on ARM CPUs as well. In order to enable these attacks in a real-world scenario we have overcome all challenges that prevented highly accurate cache attacks on ARM. Second, contrary to existing cache attacks against cryptographic primitives on ARM CPUs, our attack does not require any permissions and can be executed on any non-rooted device. Our attack works on millions of off-the-shelf Android smartphones. Furthermore, our attack is not specifically tailored for any cryptographic algorithm but instead can be used to launch cache template attacks on any target application, e.g., libraries or Android apps. More specifically, we demonstrated the immense power of the Evict+Reload attack by inferring specific user interactions with the mobile device. This includes touch and swipe actions on the screen, touch actions on the soft-keyboard, and inter-keystroke timings. In addition we present an efficient key-recovery attack on the default AES implementation that is part of the Java Bouncy Castle library.

The presented example attacks are by no means exhaustive and launching our proposed attack against other libraries and apps will reveal further exploitable information leaks. Thus, our findings stress the urgent need to deploy effective countermeasures in order to protect millions of Android users from being attacked.

REFERENCES


